ALESIS
IO|2 (UB0)
Service Manual

P/N: 8-31-0137-A

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Preface

This document is intended to assist the service technician in the operation, maintenance and repair of the Alesis device. Together with the User Reference Manual, this document provides a complete description of the functionality and serviceability of the Device. Any comments or suggestions you may have pertaining to the document are welcome and encouraged.

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Warnings

TO REDUCE THE RISK OF ELECTRIC SHOCK OR FIRE, DO NOT EXPOSE THIS PRODUCT TO WATER OR MOISTURE.



The arrowhead symbol on a lightning flash inside a triangle is intended to alert the user to the presence of un-insulated "dangerous voltage" within the enclosed product which may be of sufficient magnitude to constitute a risk of electric shock to persons.



The exclamation point inside a triangle is intended to alert the user to the presence of important operating, maintenance and servicing instructions in the literature which accompanies the product.

REPAIR BY ANY PERSON OR ENTITY OTHER THAN AN AUTHORIZED ALESIS SERVICE CENTER WILL VOID THE ALESIS WARRANTY.

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Regarding the Power Supply Fuse



CAUTION: The product under service may employ the use of a replaceable fuse. Danger of fire or electrocution if fuse is incorrectly replaced. Replace with only the same type or equivalent type recommended by the equipment manufacturer.

Regarding the Internal Battery



CAUTION: The product under service may employ the use of a internal battery. Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instruction.

Safety Instructions

Carefully read the applicable items of the operating instructions and these safety suggestions before using this product. Use extra care to follow the warnings written on the product itself and in the operating instructions. Keep the operating instructions and safety suggestions for reference in the future.

1. Power Source. The product should only be connected to a power supply which is described either in the operating instructions or in markings on the product.

2. Power Cord Protection. AC power supply cords should be placed such that no one is likely to step on the cords and such that nothing will be placed on or against them.

3. Periods of Non-use. If the product is not used for any significant period of time, the product's AC power supply cord should be unplugged from the AC outlet.

4. Foreign Objects and Liquids. Take care not to allow liquids to spill or objects to fall into any openings of the product.

5. Water or Moisture. The product should not be used near any water or in moisture.

6. Heat. Do not place the product near heat sources such as stoves, heat registers, radiators or other heat producing equipment.

7. Ventilation. When installing the product, make sure that the product has adequate ventilation. Improperly ventilating the product may cause overheating, which may damage the product.

8. Mounting. The product should only be used with a rack which the manufacturer recommends. The combination of the product and rack should be moved carefully. Quick movements, excessive force or uneven surfaces may overturn the combination which may damage the product and rack combination.

9. Cleaning. The product should only be cleaned as the manufacturer recommends.

10. Service. The user should only attempt the limited service or upkeep specifically described in the operating instructions for the user. For any other service required, the product should be taken to an authorized service center as described in the operating instructions.

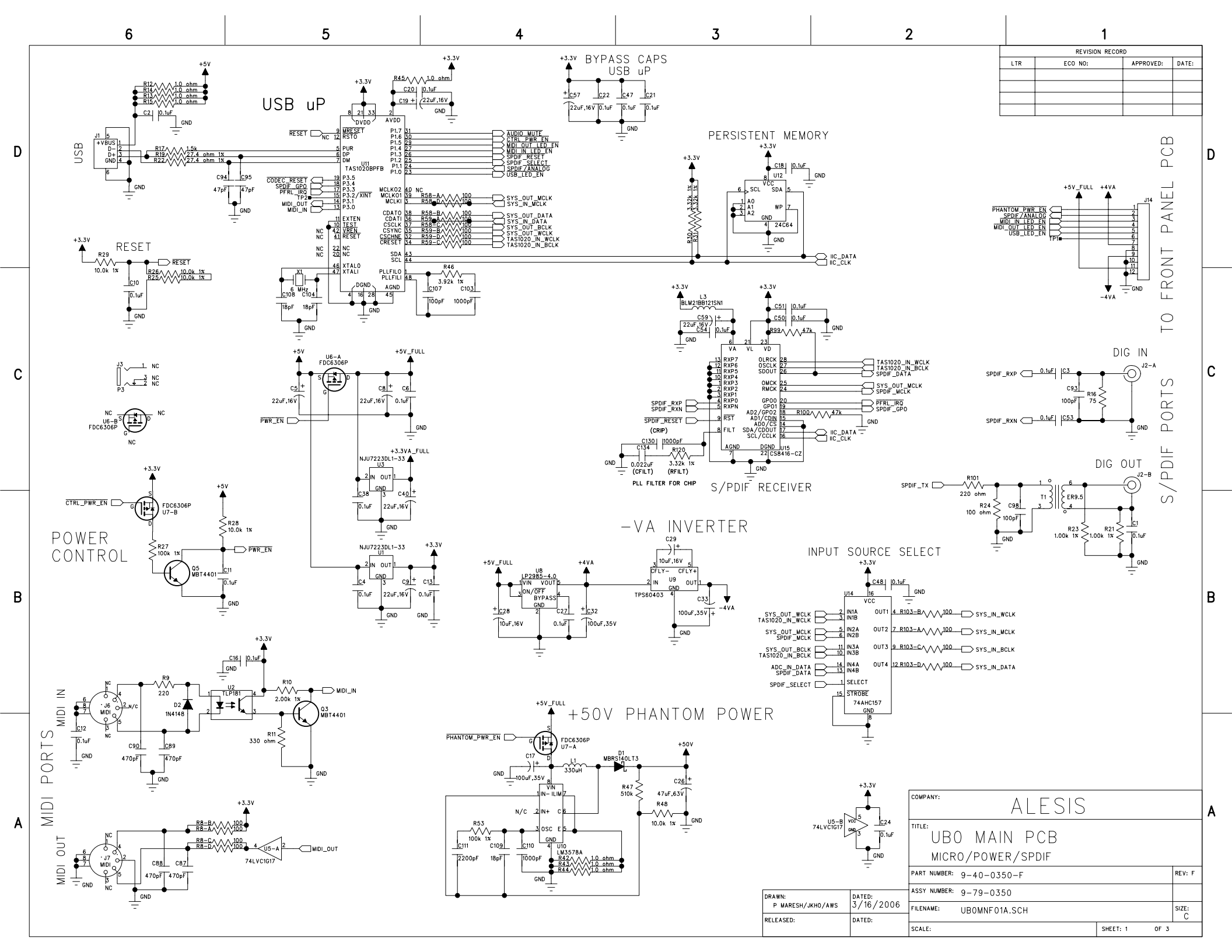
11. Damage to the Product. Qualified service personnel should service the unit in certain situations including without limitation when:
    a. Liquid has spilled or objects have fallen into the product,
    b. The product is exposed to water or excessive moisture,
    c. The AC power supply plug or cord is damaged,
    d. The product shows an inappropriate change in performance or does not operate normally, or
    e. The enclosure of the product has been damaged.

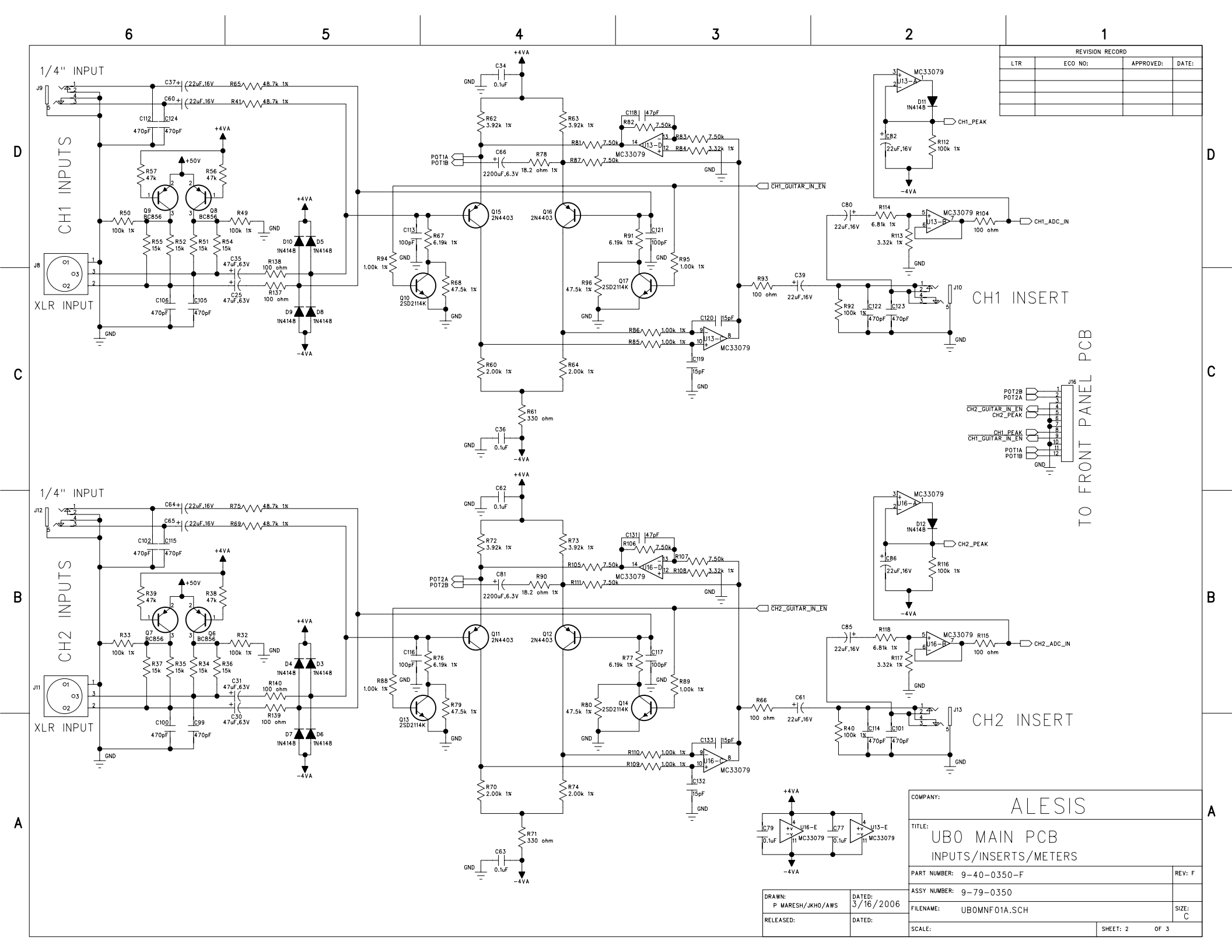
ALESIS
IO|2 (UB0)

SCHEMATIC
AND
PCB
FILES

MAIN PCB

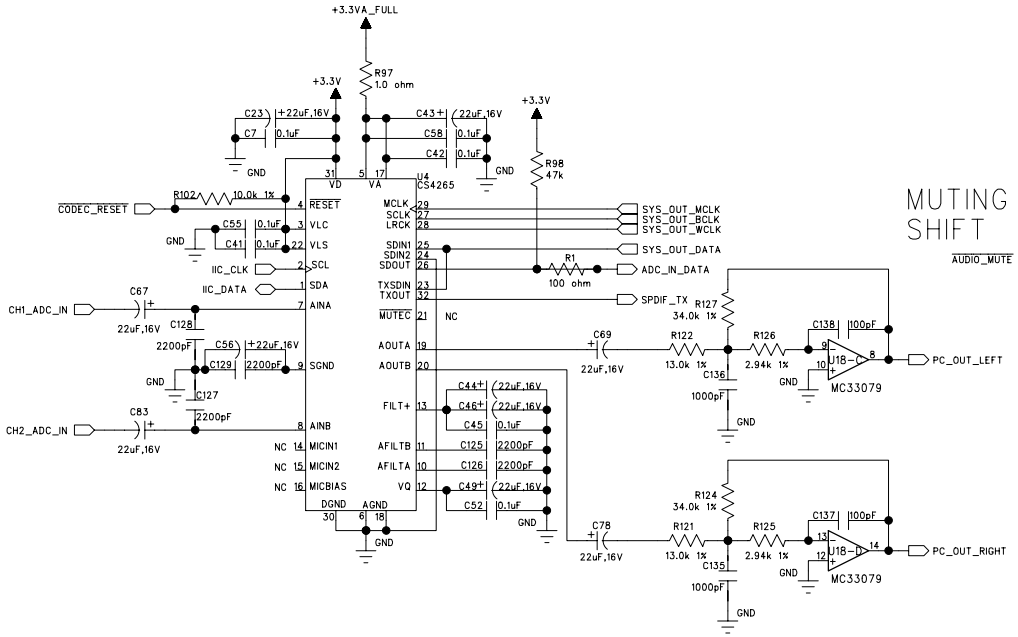
REV F


REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
USB uP
BYPASS CAPS
USB uP
PERSISTENT MEMORY
RESET
TO FRONT PANEL PCB
DIG IN
DIG OUT
S/PDIF PORTS
S/PDIF RECEIVER
PLL FILTER FOR CHIP
POWER CONTROL
-VA INVERTER
INPUT SOURCE SELECT
MIDI PORTS
MIDI IN
MIDI OUT
+50V PHANTOM POWER
ALESIS
UB0 MAIN PCB
MICRO/POWER/SPDIF
PART NUMBER: 9-40-0350-F
REV: F
ASSY NUMBER: 9-79-0350
FILENAME: UB0MNF01A.SCH
SIZE: C
SCALE:
SHEET: 1 OF 3
DRAWN: P MARESH/JKHO/AWS
DATED: 3/16/2006
RELEASED:
DATED:

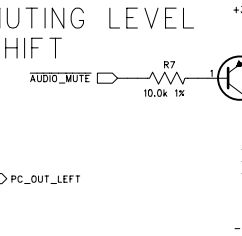

1/4" INPUT
CH1 INPUTS
XLR INPUT
CH1_GUITAR_IN_EN
CH1_PEAK
CH1_ADC_IN
CH1 INSERT
1/4" INPUT
CH2 INPUTS
XLR INPUT
CH2_GUITAR_IN_EN
CH2_PEAK
CH2_ADC_IN
CH2 INSERT
TO FRONT PANEL PCB
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
COMPANY:
ALESIS
TITLE:
UBO MAIN PCB
INPUTS/INSERTS/METERS
PART NUMBER: 9-40-0350-F
REV: F
ASSY NUMBER: 9-79-0350
FILENAME: UBOMNF01A.SCH
SIZE: C
SCALE:
SHEET: 2 OF 3
DRAWN: P MARESH/JKHO/AWS
DATED: 3/16/2006
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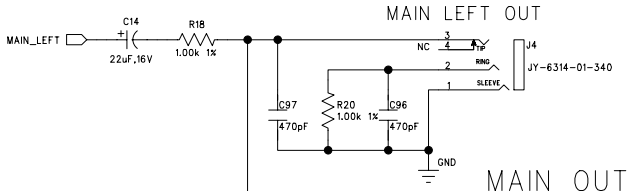
SPDIF OUT
CH1/2 IN ADC, PC OUT DAC



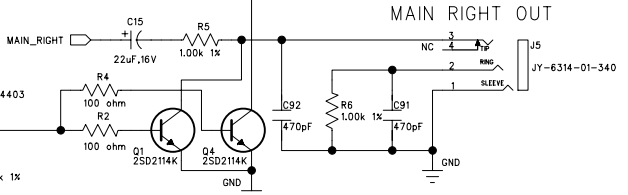
MUTING LEVEL SHIFT



MAIN LEFT OUT

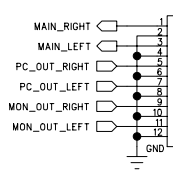


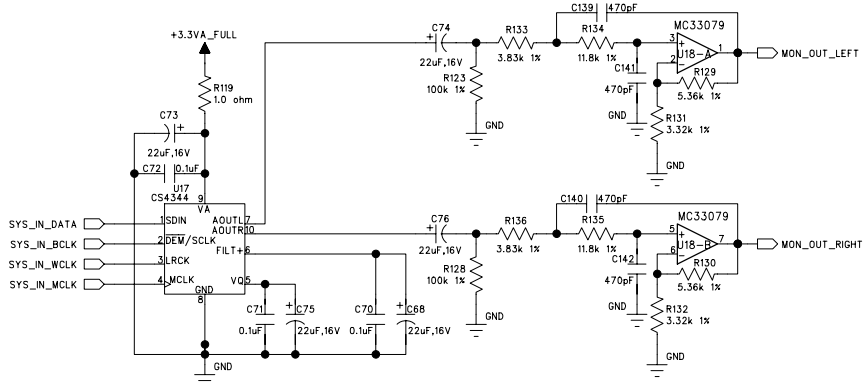
MAIN RIGHT OUT



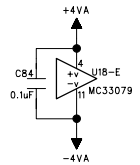
MAIN OUTS

TO FRONT PANEL PCB



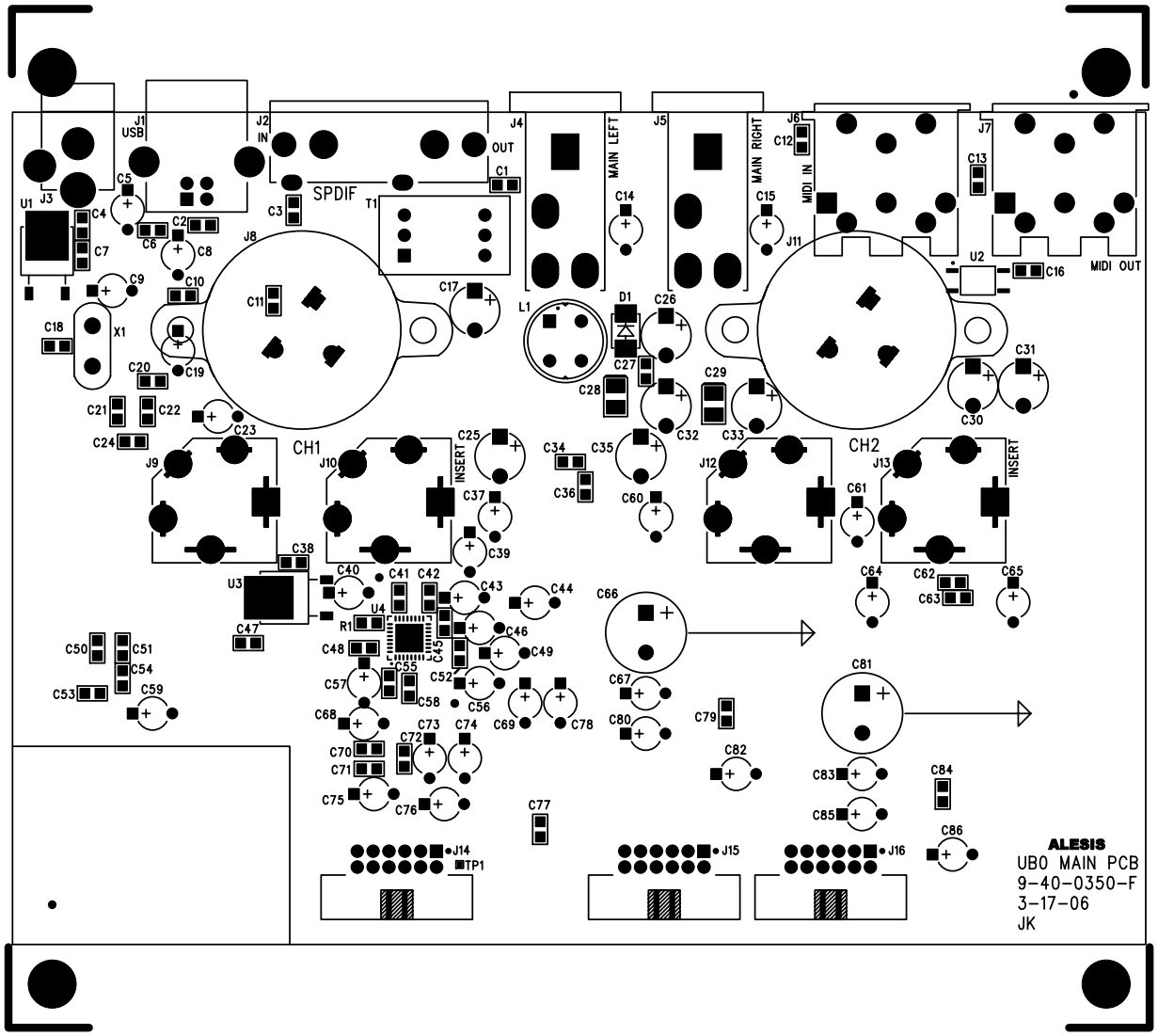


MONITOR DAC



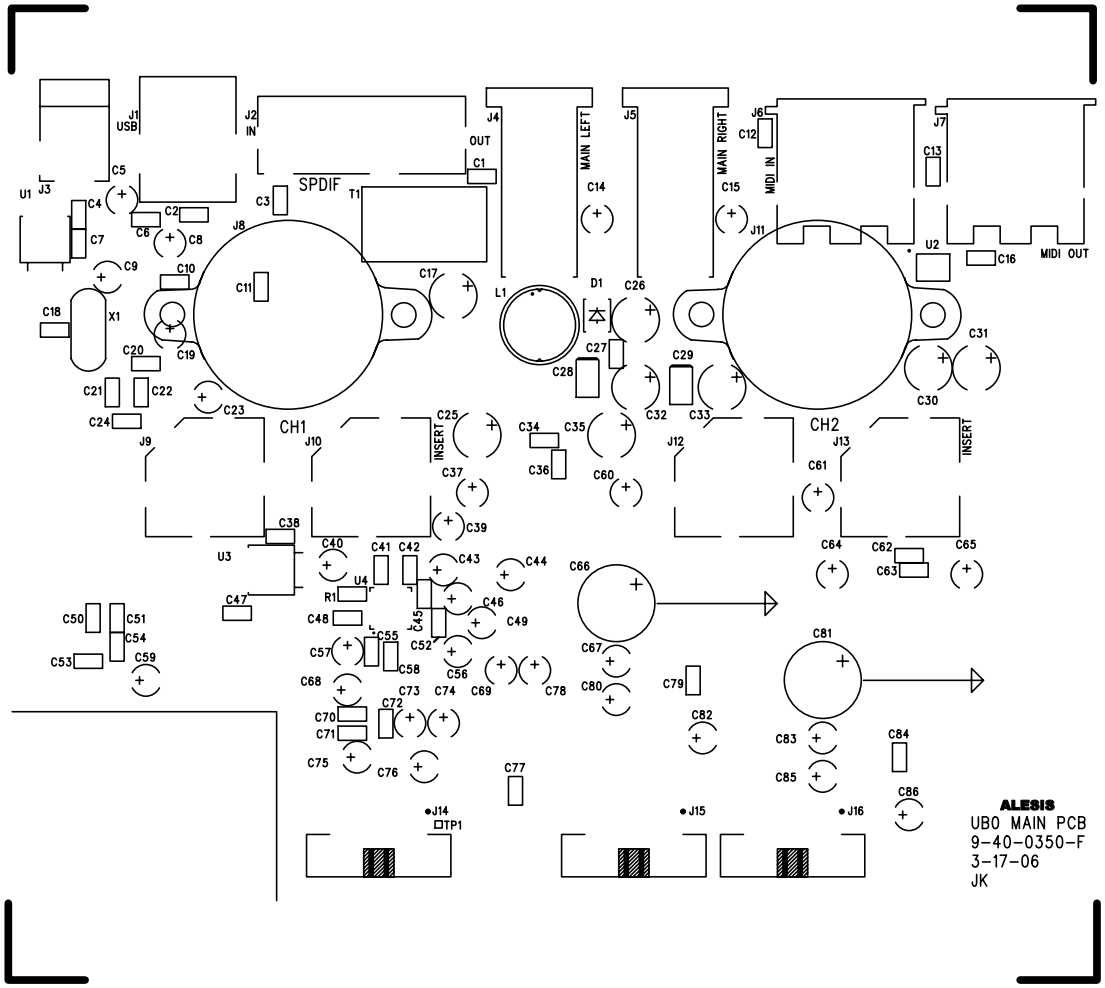
COMPANY:	ALESIS		
TITLE:	UBO MAIN PCB OUTPUTS/CONVERTERS		
PART NUMBER:	9-40-0350-F		REV: F
ASSY NUMBER:	9-79-0350		
FILENAME:	UBOMNF01A.SCH		SIZE: C
SCALE:		SHEET: 3 OF 3	
DRAWN: P MARESH/JKHO/AWS	DATED: 3/16/2006		
RELEASED:	DATED:		

ALESIS 9-79-0350-F "TOP ASSEMBLY DRAWING"





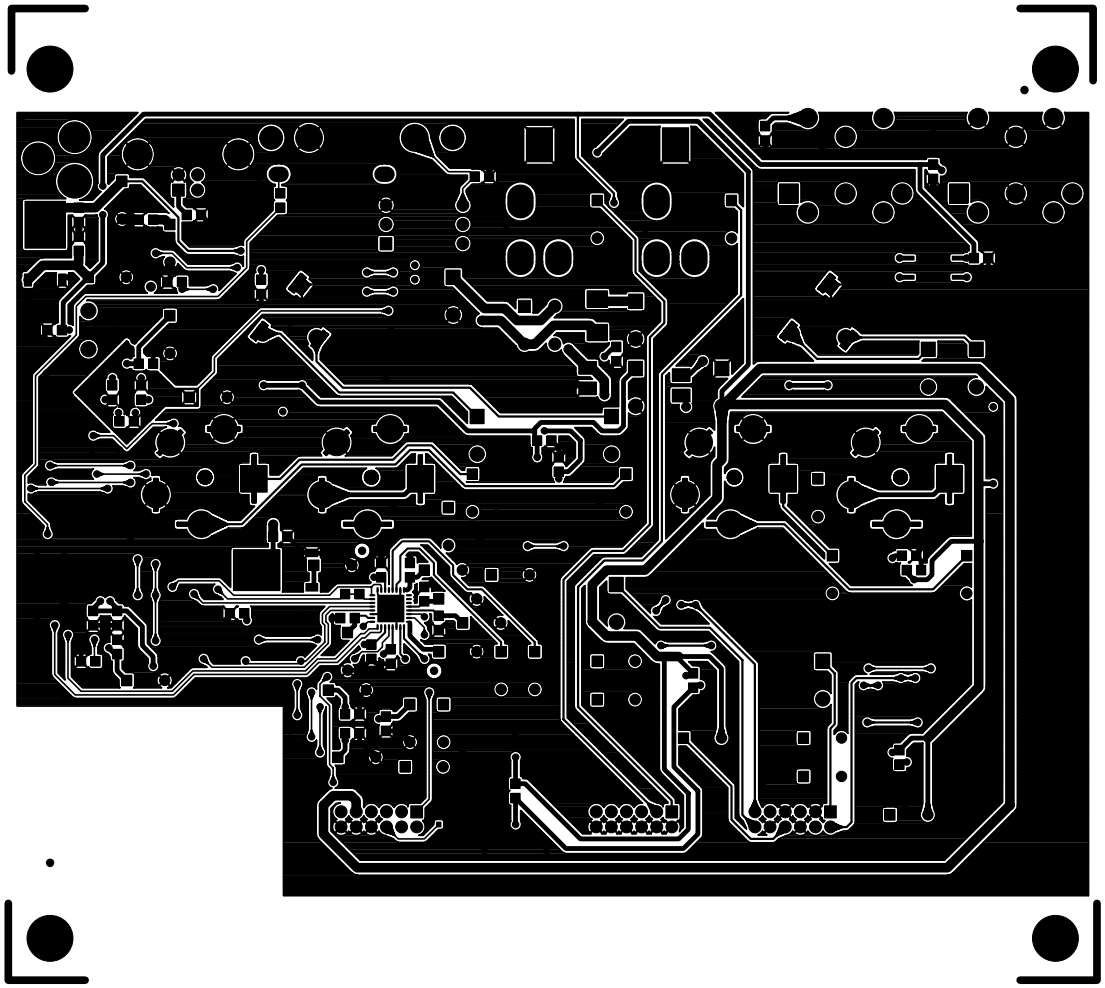
ALESIS 9-40-0350-F "TOPPASTE"



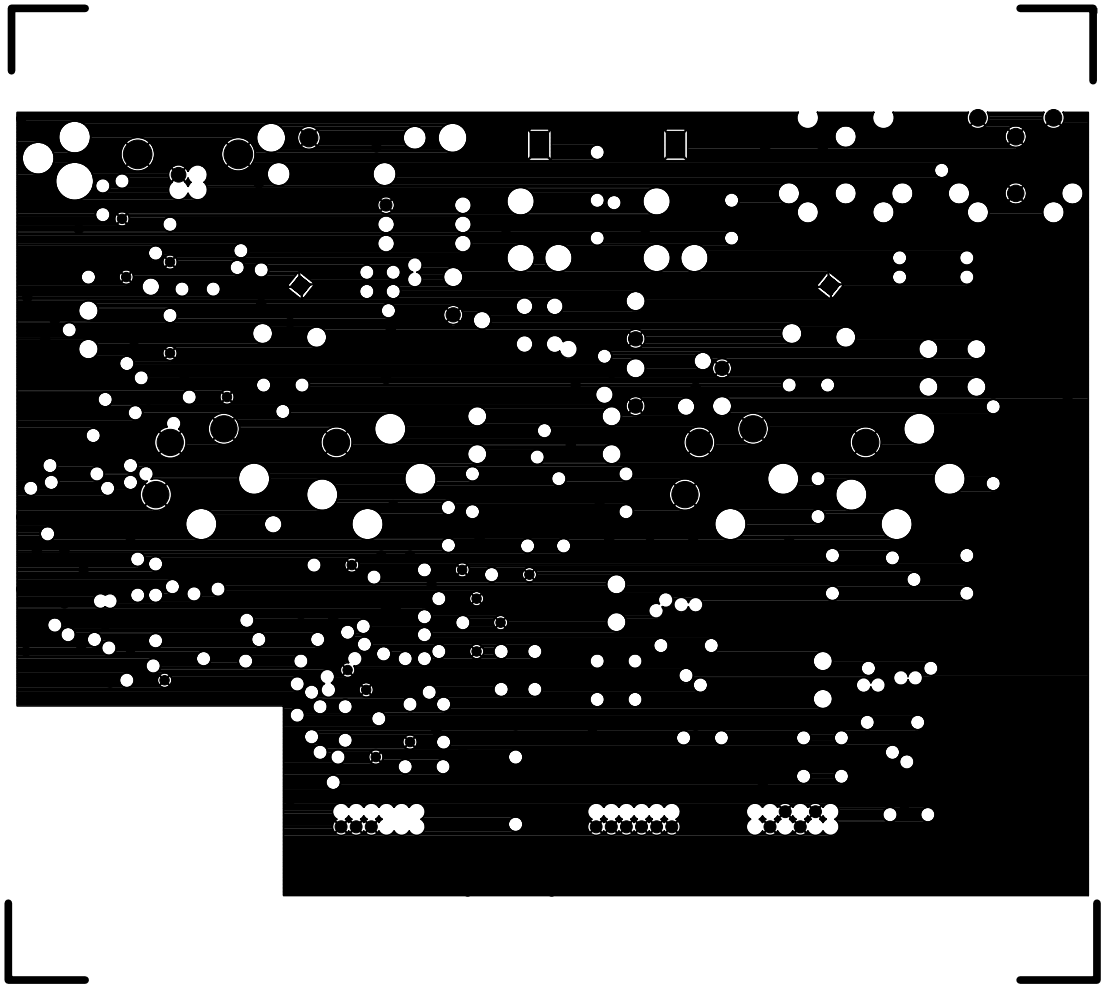
ALESIS 9-40-0350-F "TOPSILK"



ALESIS 9-40-0350-F "TOPSMK"

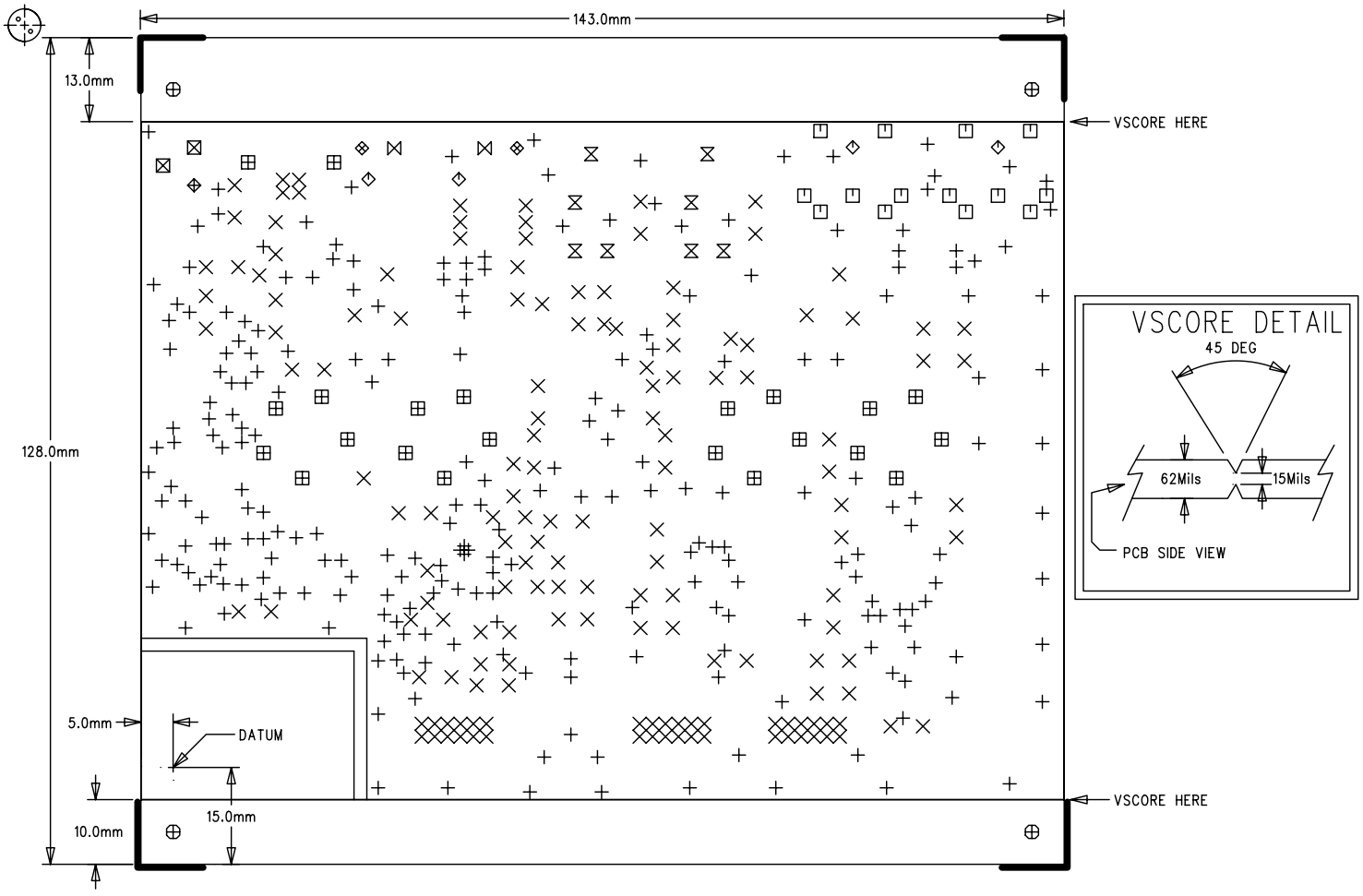


ALESIS 9-40-0350-F "TOPTRACE"



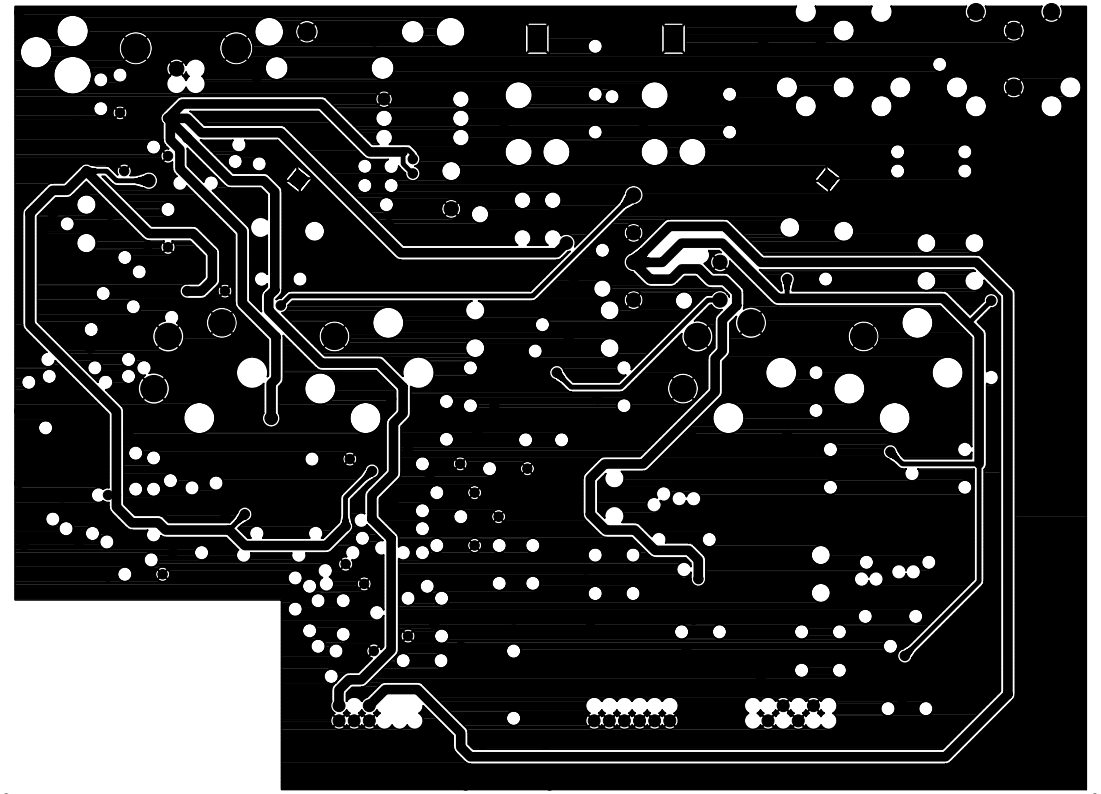
ALESIS 9-40-0350-F "GNDPLANE LAYER 2"

ALESIS 9-40-0350-F "DRILLDWG"

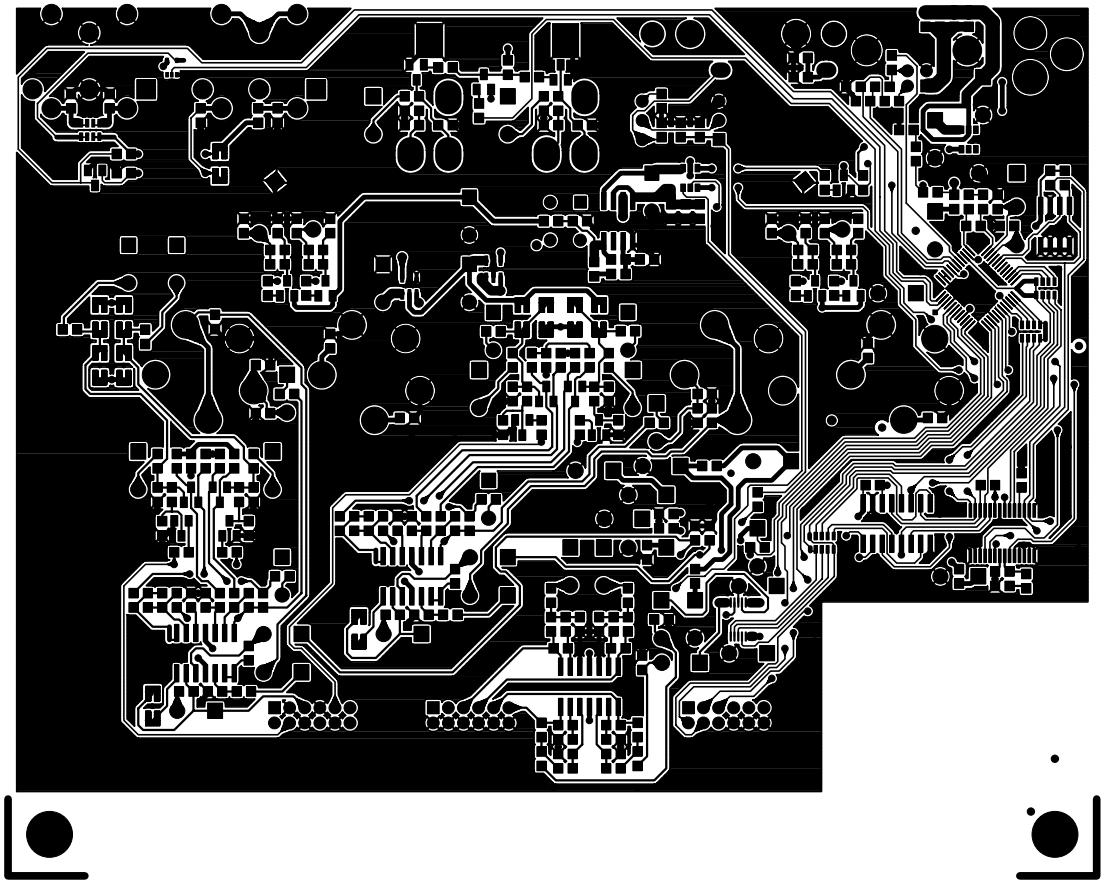


SIZE	QTY	SYM	PLATED	TOL
20	242	+	YES	+/-3
37	153	X	YES	+/-3
43.3	14	square	YES	+/-3
49.2	4	diamond	YES	+/-3
82.7	8	hourglass	YES	+/-3
86.6	2	bowtie	YES	+/-3
90.6	22	square+	YES	+/-3
100.4	2	square X	YES	+/-3
125	1	diamond+	YES	+/-3
126	2	diamond X	NO	+/-3
157.5	4	circle+	NO	+/-3

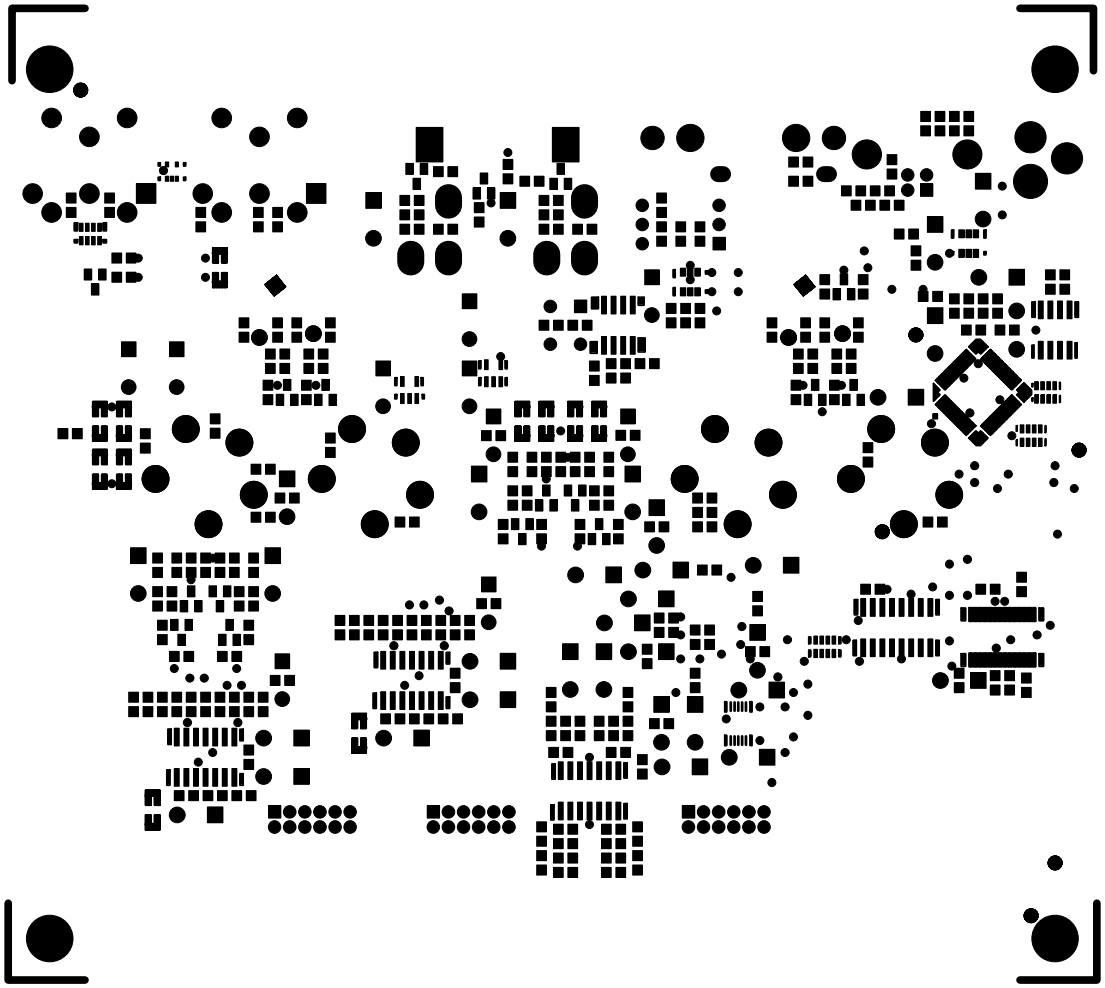
1. Design rules used: 0.008" lines. 0.008" space
2. 4-layer design.
3. Surface-mount parts on top and bottom sides.
4. Material: 0.062" (+/- 0.007") thick glass epoxy FR-4 (green) 1 oz. copper all layers, finished.
5. Finish: Must be lead free. SMOBC (HASL) if available.
6. Hole sizes are finished diameter after plating with 0.0010" minimum plating all surfaces. (Except 20 mil via which MAY be plated closed.) Drilled holes are +/- 0.003" tolerance.
7. Layer-to-layer registration to be +/-0.005"
8. Soldermask all exposed copper, LPI, GREEN color.
9. Silkscreen using epoxy-based ink (white).
10. Surface to be flat within 0.010" in/in of diagonal measurement.
11. Vendor shall etch, silkscreen or stamp I.D. logo and date code, type designation and UL flame rating on top side of PCB. NO COPPER MAY BE DELETED
12. Soldercoat both sides to standard J-STD-003.
13. Finished pcb shall have 0.0035" min dielectric material between consecutive conductor layers when cured.
14. Mechanical dims are +/- 0.005" tolerance.
15. Workmanship and acceptance criteria shall be in accordance with IPC-A-600, Class 1.



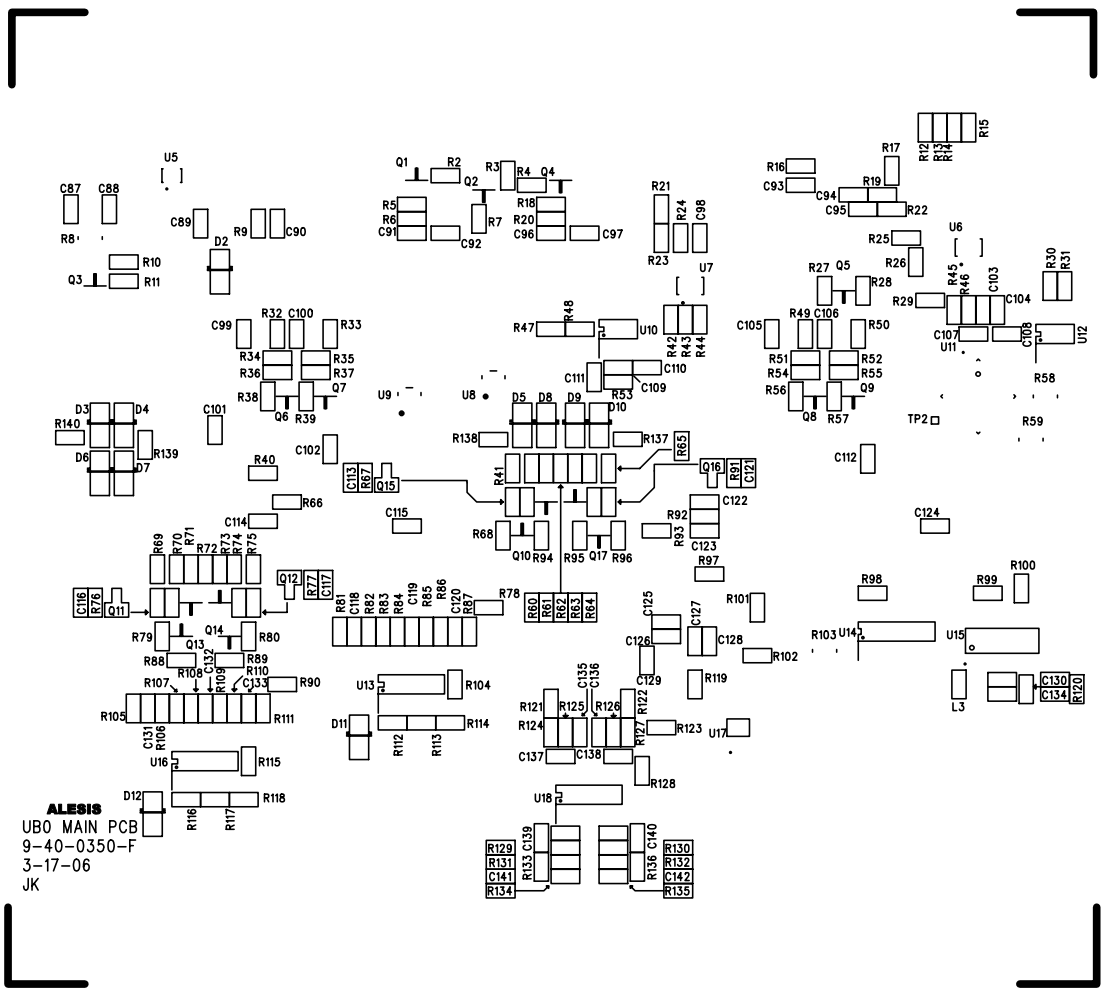
ALESIS 9-40-0350-F "PWRPLANE LAYER 3"



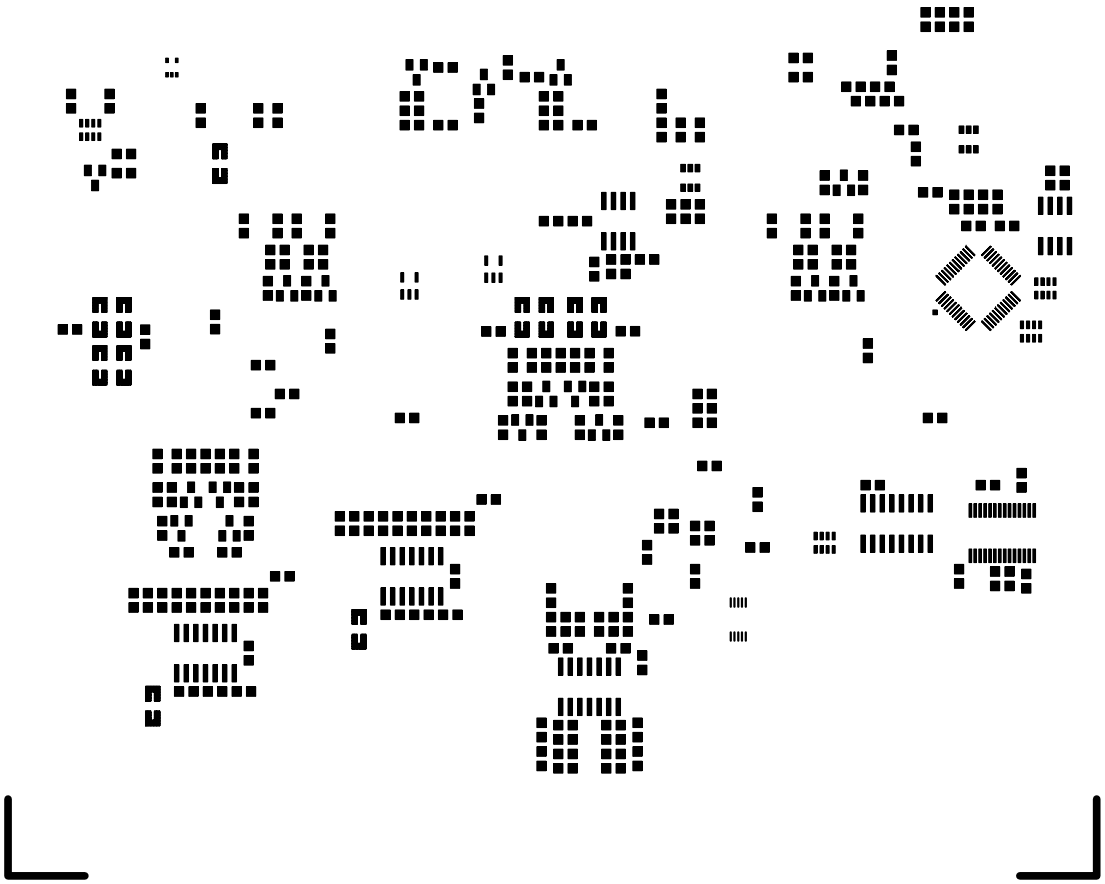
ALESIS 9-40-0350-F "BOTTRACE"



ALESIS 9-40-0350-F "BOTSMK"

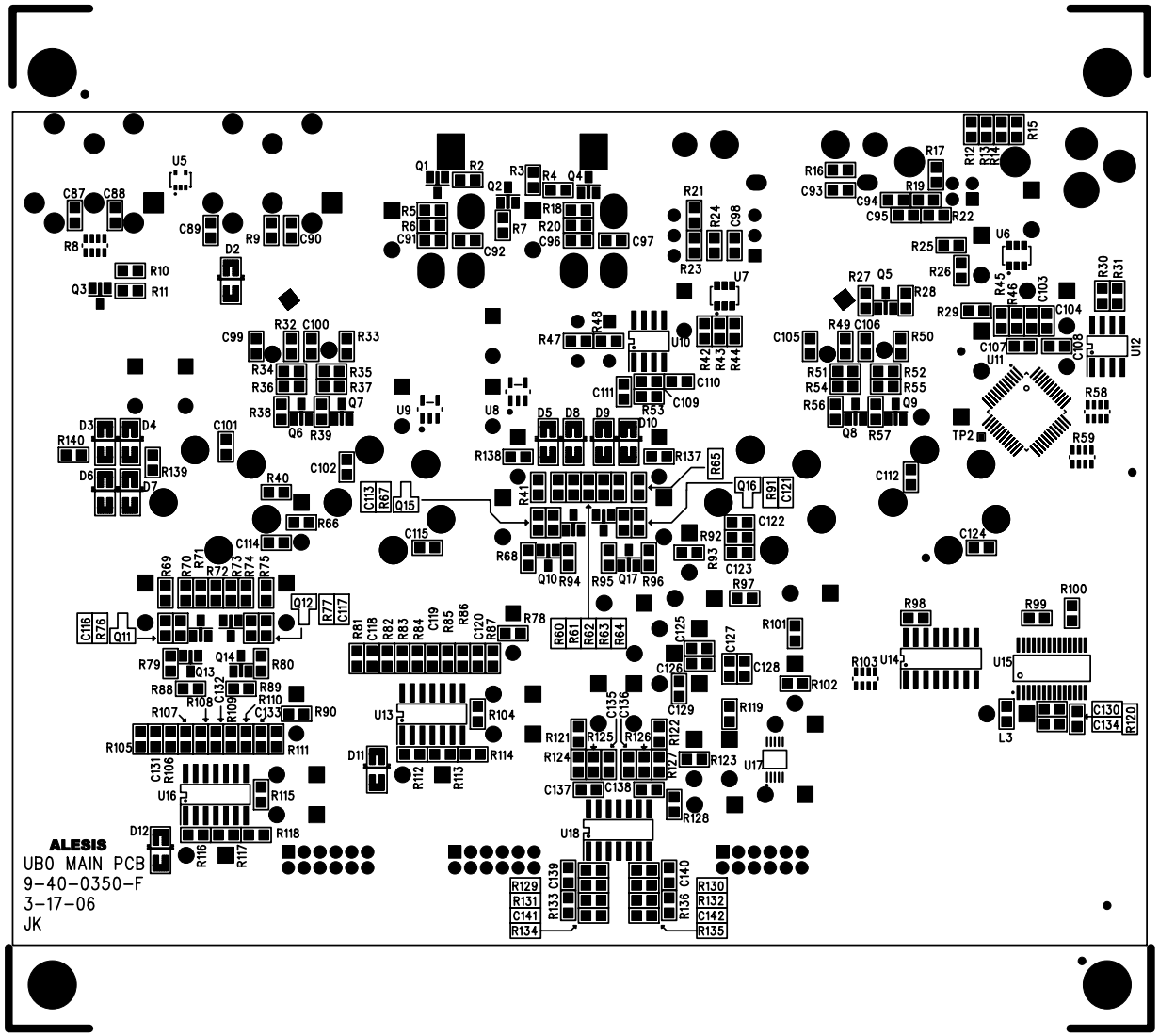


ALESIS 9-40-0350-F "BOTSILK"



ALESIS 9-40-0350-F "BOTPASTE"

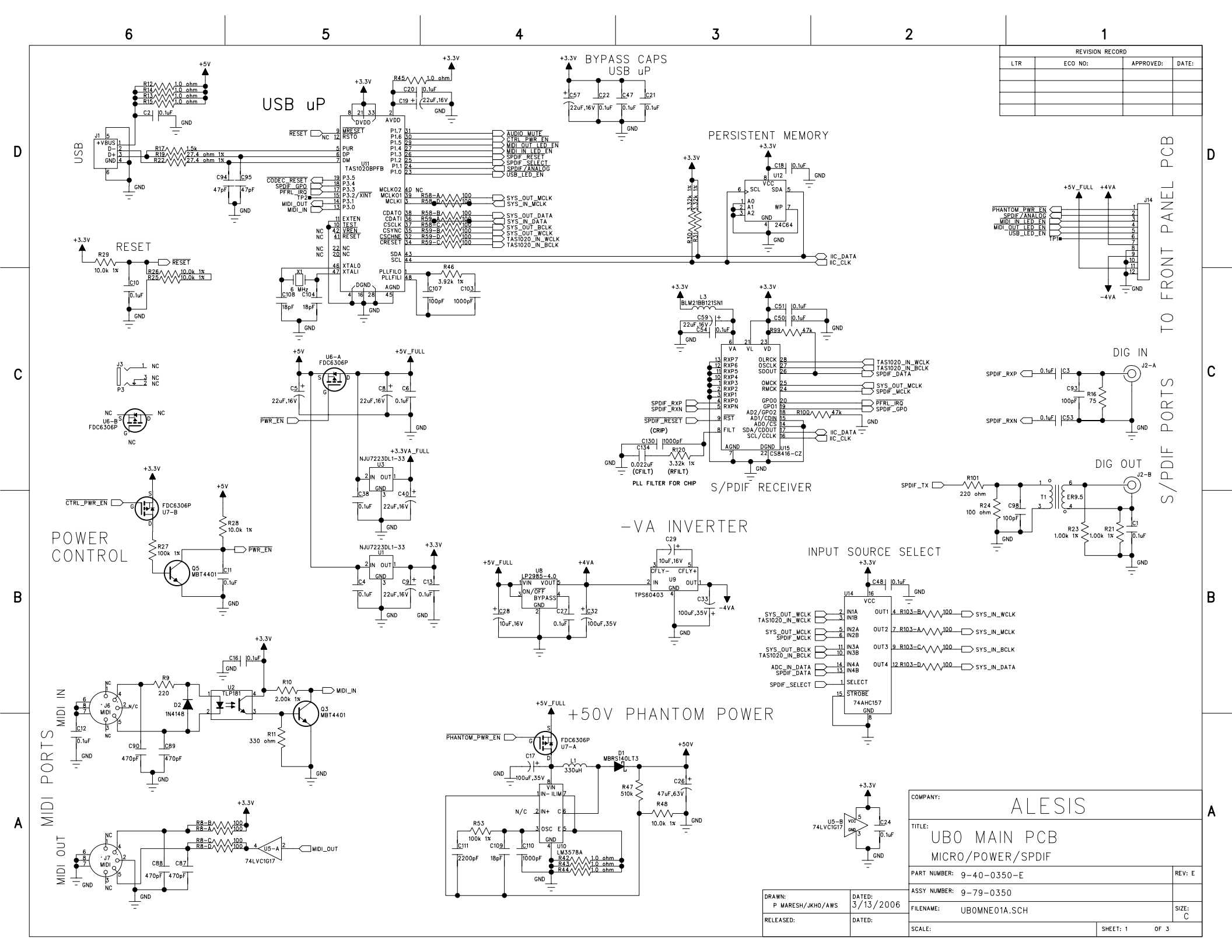
ALESIS 9-79-0350-F "BOTTOM ASSEMBLY DRAWING"

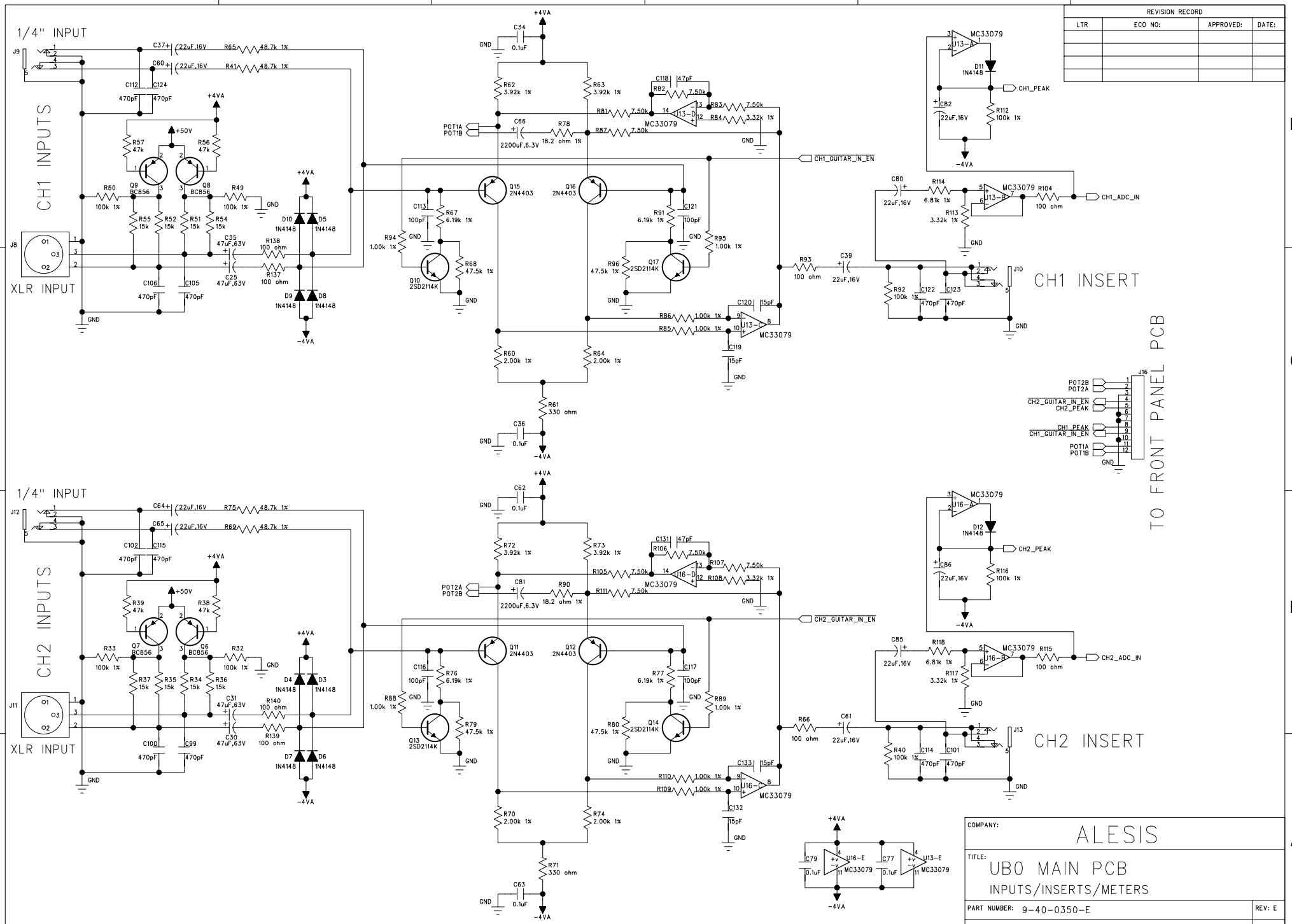


	UB0MNF - Main PCB Rev F						**Last Revised:**	
	RevChange Document						**3/17/2006**	
SCH	**PCB**	**CAM**	**Suggested by:**	**DATE**	**Performed by:**	**DATE**	**Description of change:**	**Reason for change:**
							TOP LEVEL CHANGES	
x	x		SOP	3/13/2006	JK	3/17/2006	Change all text from Rev E to F	SOP
			SOP	3/13/2006			update all Part Types	SOP
			SOP	3/13/2006			Review/Integrate all outstanding ECNs	SOP
							Note: ***A new solderpaste stencil IS NOT required***	No SMD components were moved.
							SCHEMATIC CHANGES	
							PCB CHANGES	
	x		JK	3/14/2006	JK	3/17/2006	Flood power plane.	
	x		YH	3/16/2006	JK	3/16/2006	The bottom layer pads of C75's negative terminal and C76's positive terminal are too close.	The leads of the thru-hole components at these locations, after being bent during the auto-insertion process (to prevent the components from falling out), tend to short out against the neighboring pads during the wave-solder process.
	x		YH	3/16/2006	JK	3/16/2006	The bottom layer pads of C43's negative terminal and C44's positive terminal are too close.	
	x		YH	3/16/2006	JK	3/16/2006	The bottom layer pads of C57's negative terminal and C68's positive terminal are too close.	
	x		YH	3/16/2006	JK	3/16/2006	The bottom layer pad of C40's negative terminal is too close to C41's +3.3V via.	
	x		YH	3/16/2006	JK	3/16/2006	The bottom layer pad of C60's negative terminal is too close to one of R68's pads.	

MAIN PCB

REV E


REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
USB uP
BYPASS CAPS
USB uP
PERSISTENT MEMORY
RESET
TO FRONT PANEL PCB
DIG IN
DIG OUT
S/PDIF PORTS
S/PDIF RECEIVER
PLL FILTER FOR CHIP
POWER CONTROL
-VA INVERTER
INPUT SOURCE SELECT
MIDI PORTS
MIDI IN
MIDI OUT
+50V PHANTOM POWER
ALESIS
UBO MAIN PCB
MICRO/POWER/SPDIF
COMPANY:
TITLE:
PART NUMBER: 9-40-0350-E
REV: E
ASSY NUMBER: 9-79-0350
FILENAME: UBOMNE01A.SCH
SIZE: C
SCALE:
SHEET: 1 OF 3
DRAWN: P MARESH/JKHO/AWS
DATED: 3/13/2006
RELEASED:
DATED:



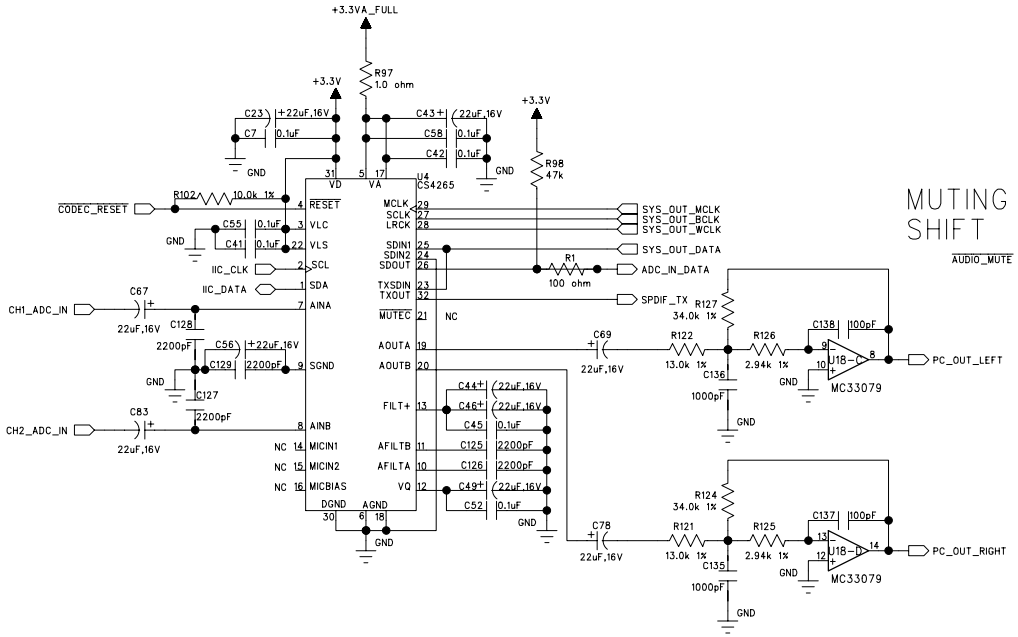
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

COMPANY:	ALESIS	
TITLE:	UBO MAIN PCB INPUTS/INSERTS/METERS	
PART NUMBER:	9-40-0350-E	REV: E
ASSY NUMBER:	9-79-0350	
FILENAME:	UBOMNE01A.SCH	SIZE: C
SCALE:	SHEET: 2 OF 3	

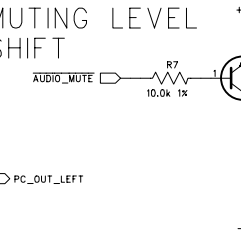
DRAWN: P MARESH/JKHO/AWS	DATED: 3/13/2006
RELEASED:	DATED:

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

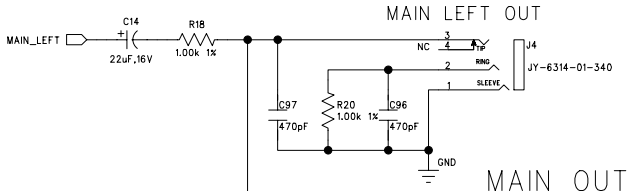
SPDIF OUT
CH1/2 IN ADC, PC OUT DAC



MUTING LEVEL SHIFT

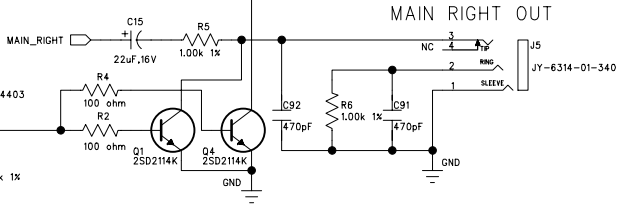


MAIN LEFT OUT

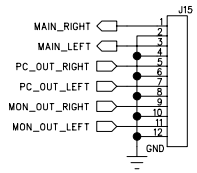


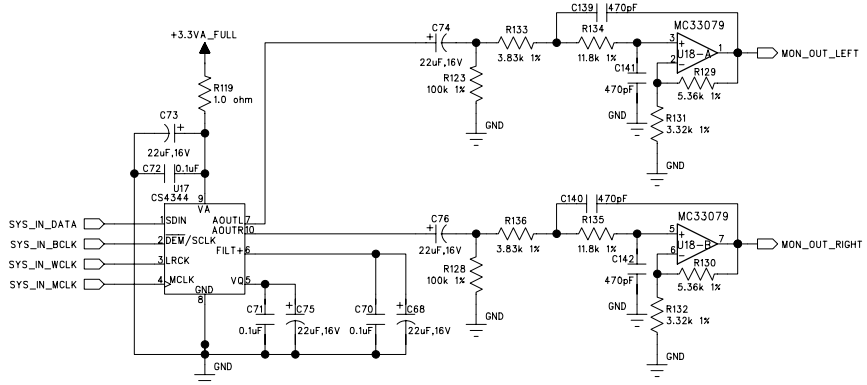
MAIN OUTS

MAIN RIGHT OUT

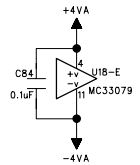


TO FRONT PANEL PCB



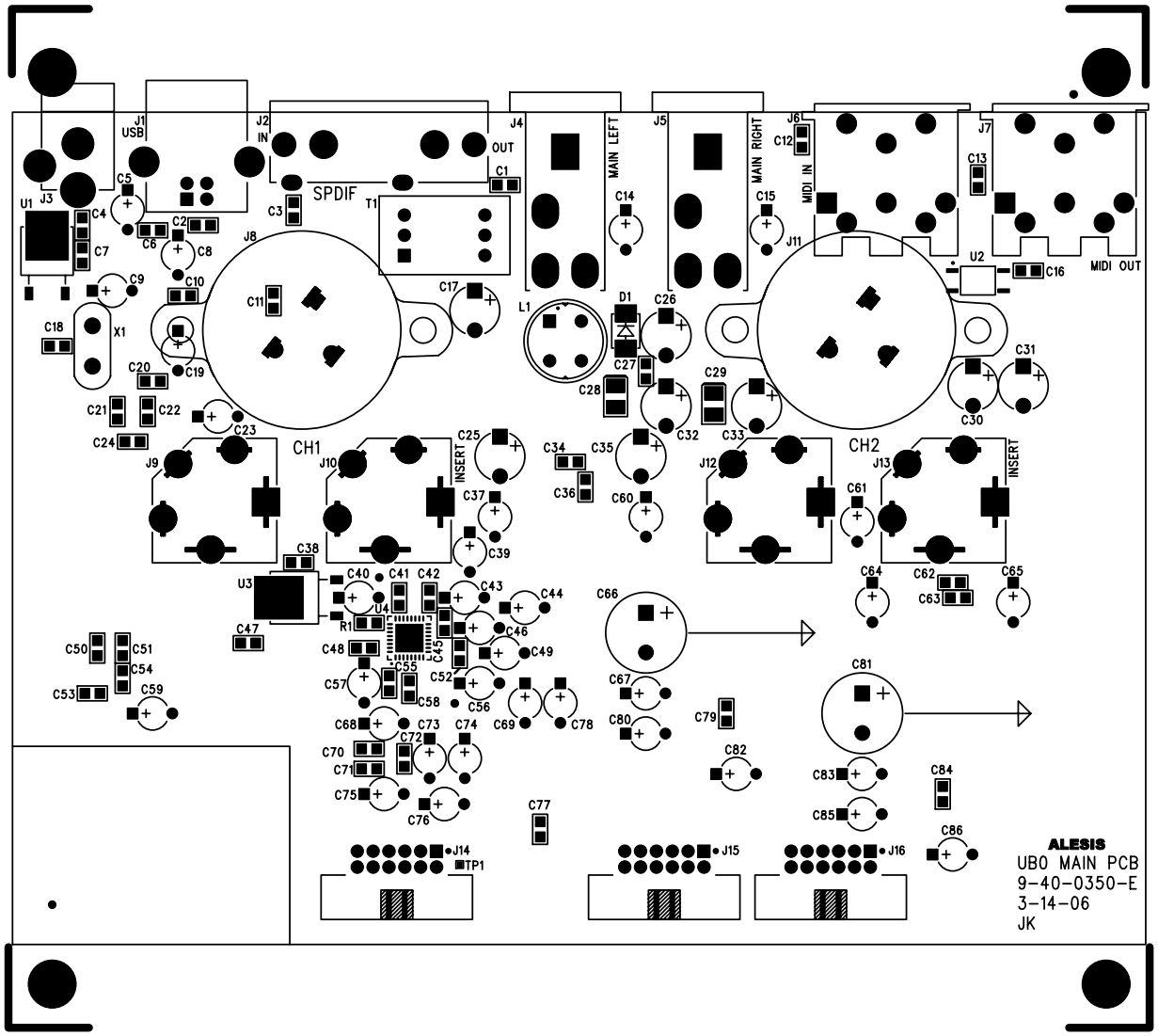


MONITOR DAC



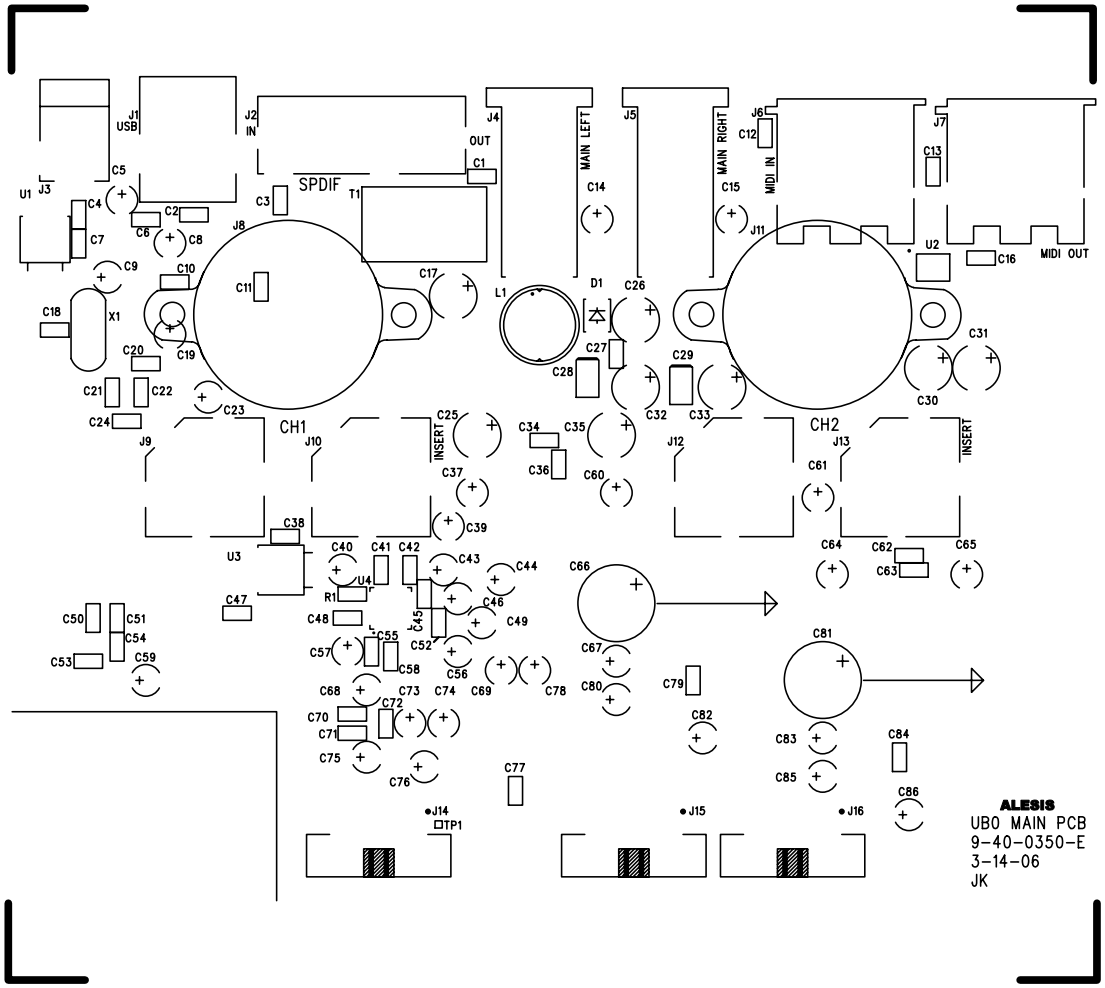
DRAWN: P MARESH/JKHO/AWS	DATED: 3/13/2006	COMPANY: ALESIS	
RELEASED:	DATED:	TITLE: UBO MAIN PCB OUTPUTS/CONVERTERS	
		PART NUMBER: 9-40-0350-E	REV: E
		ASSY NUMBER: 9-79-0350	
		FILENAME: UBOMNE01A.SCH	SIZE: C
		SCALE:	SHEET: 3 OF 3

ALESIS 9-79-0350-E "TOP ASSEMBLY DRAWING"





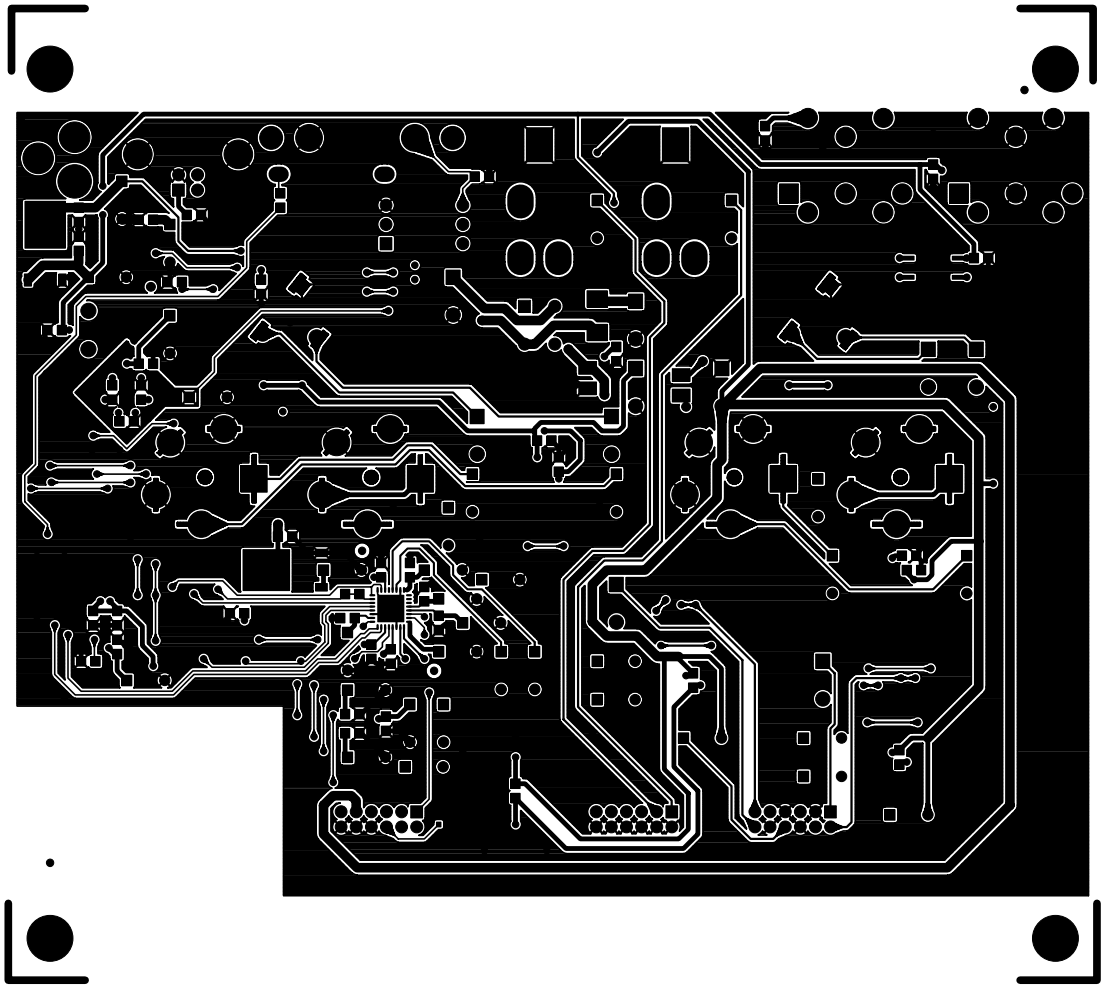
ALESIS 9-40-0350-E"TOPPASTE"



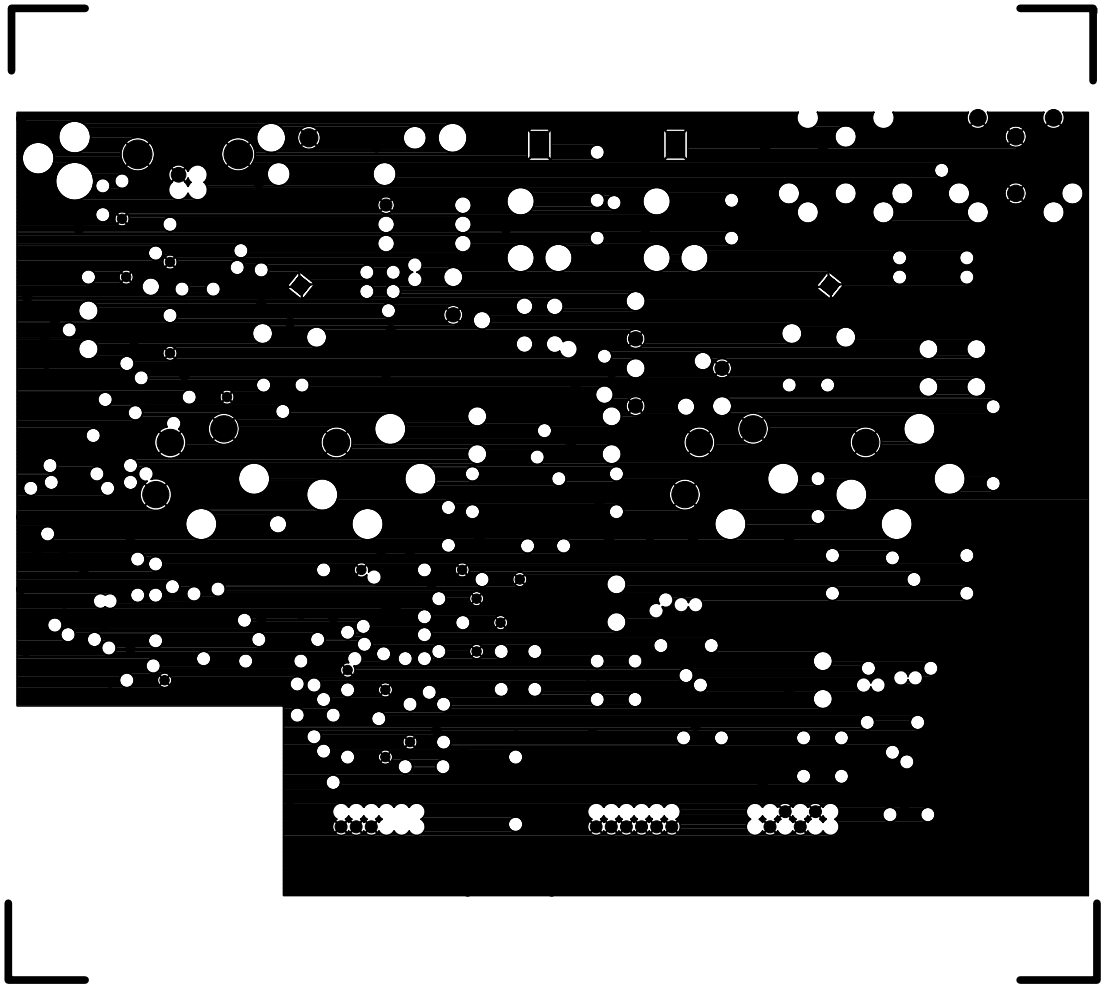
ALESIS 9-40-0350-E "TOPSILK"



ALESIS 9-40-0350-E "TOPSMK"

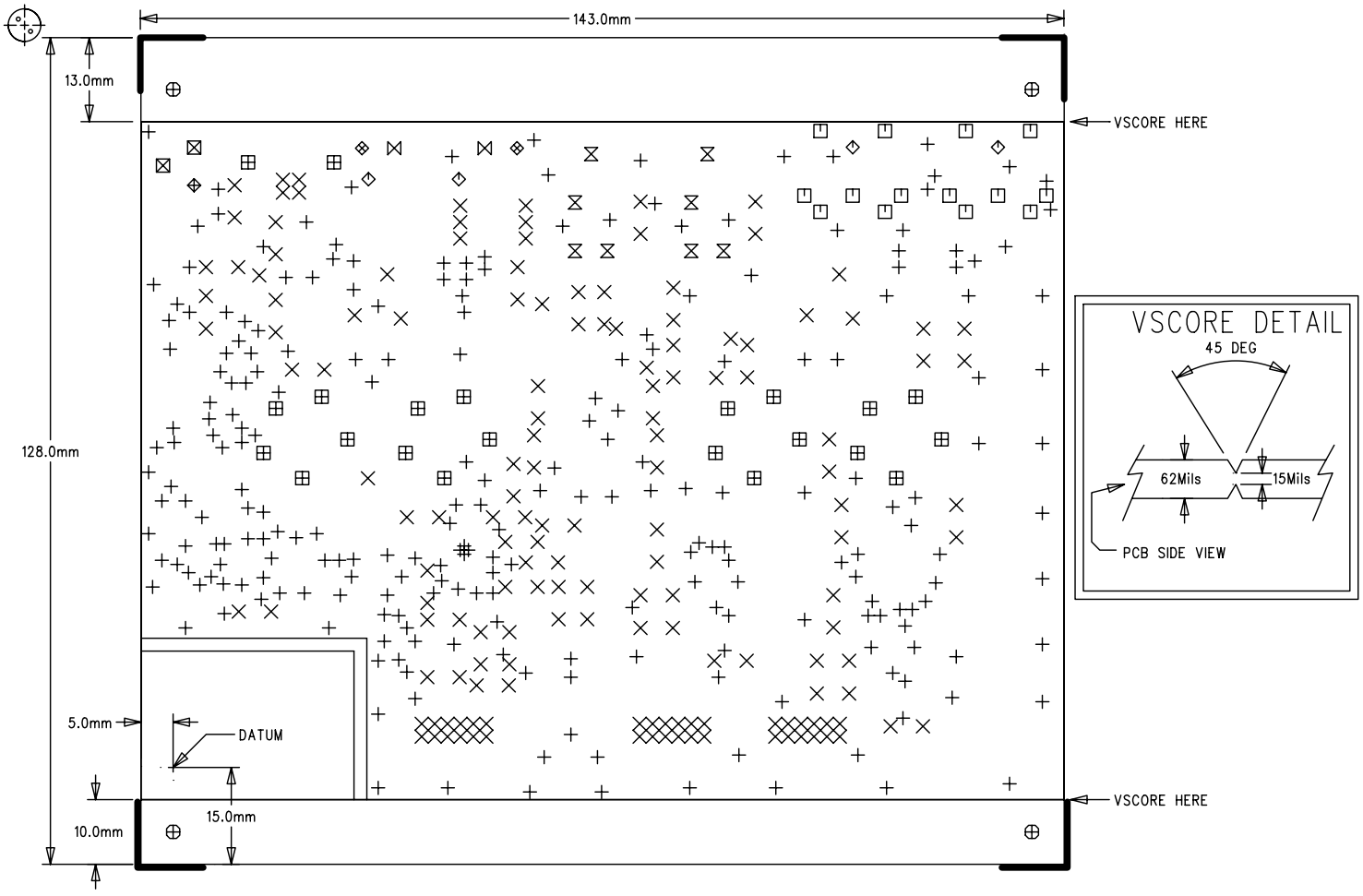


ALESIS 9-40-0350-E "TOPTRACE"



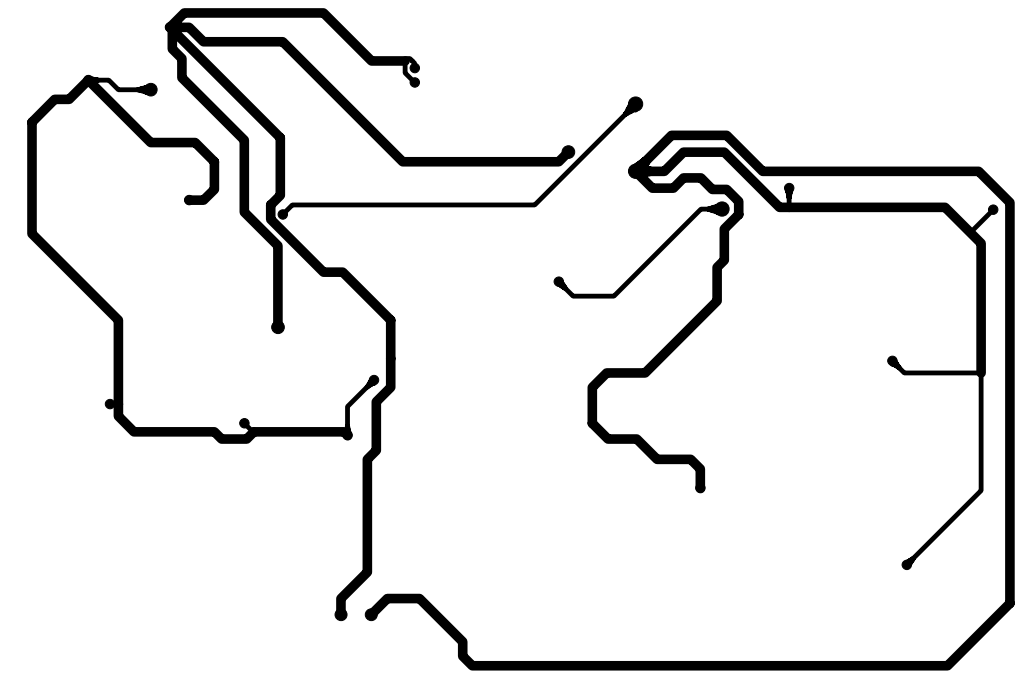
ALESIS 9-40-0350-E "GNDPLANE LAYER 2"

ALESIS 9-40-0350-E "DRILLDWG"

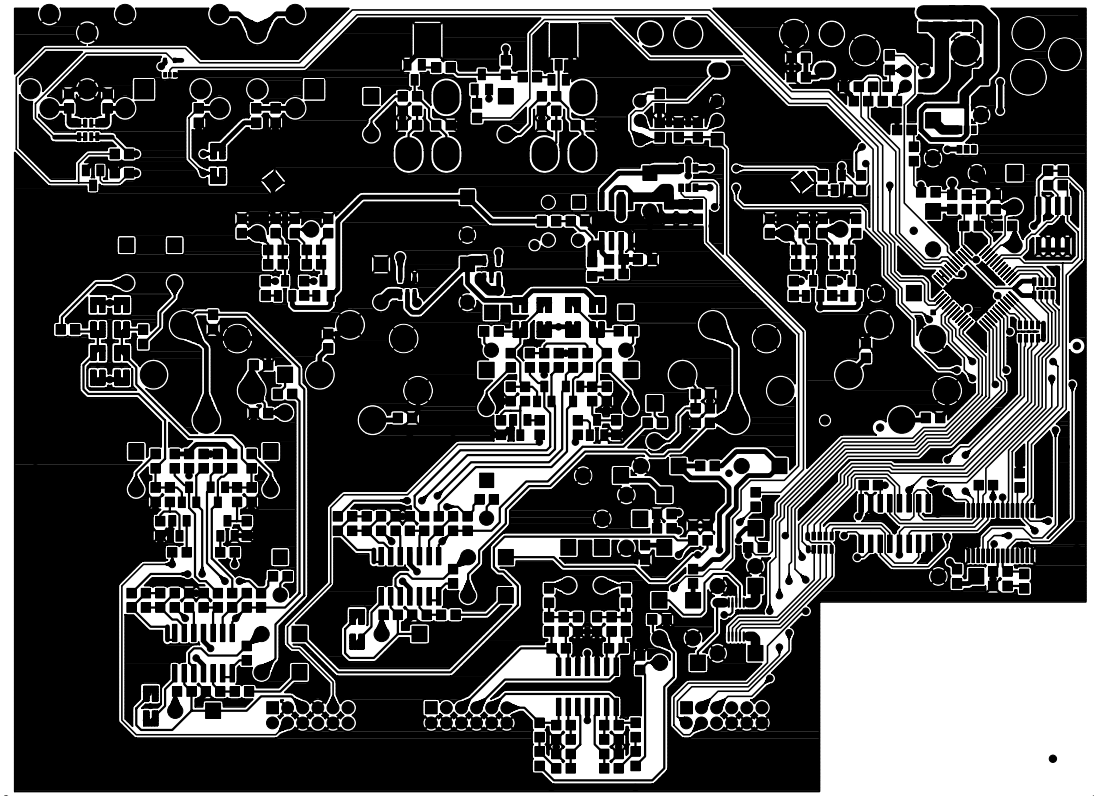


SIZE	QTY	SYM	PLATED	TOL
20	241	+	YES	+/-3
37	153	X	YES	+/-3
43.3	14	□	YES	+/-3
49.2	4	◇	YES	+/-3
82.7	8	⧖	YES	+/-3
86.6	2	⋈	YES	+/-3
90.6	22	⊞	YES	+/-3
100.4	2	⊠	YES	+/-3
125	1	⧫	YES	+/-3
126	2	◈	NO	+/-3
157.5	4	⊕	NO	+/-3

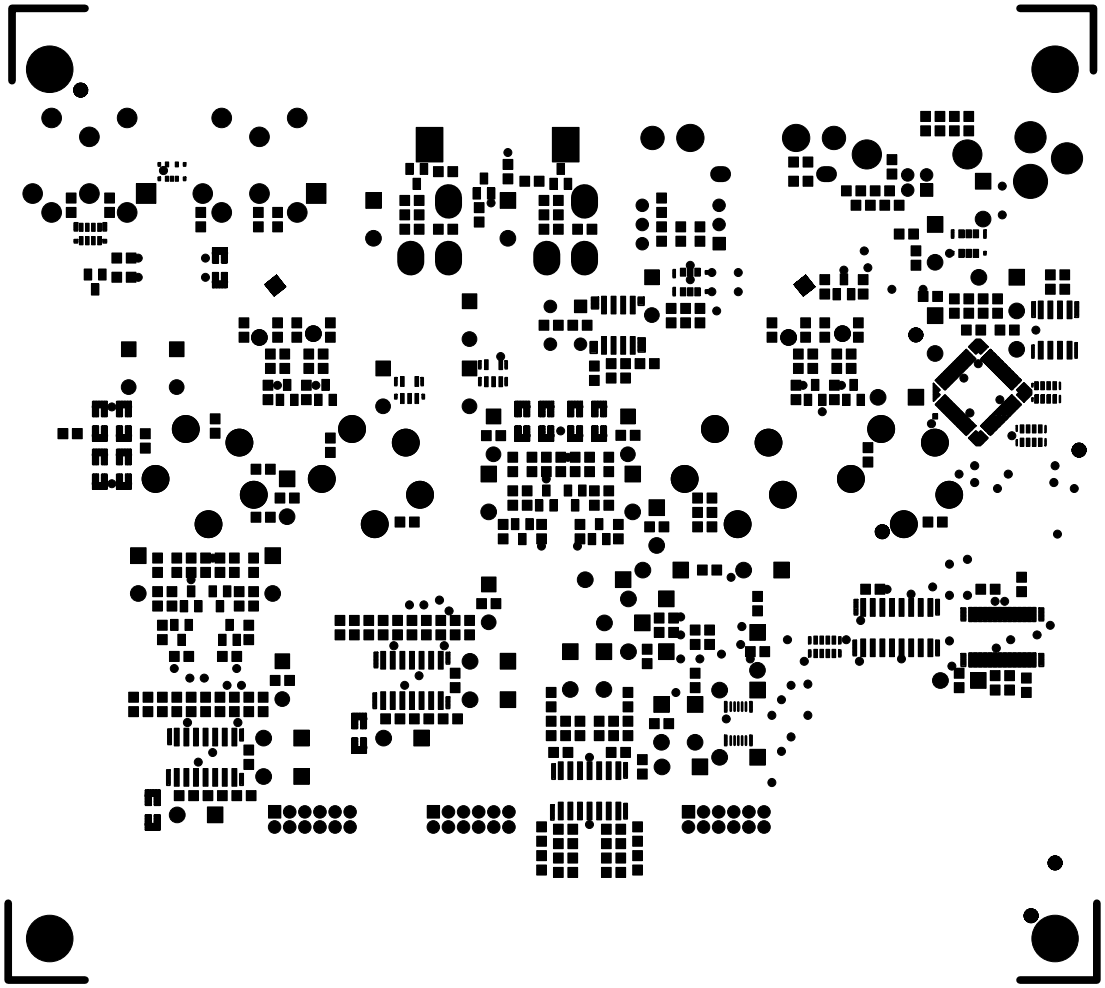
1. Design rules used: 0.008" lines. 0.008" space
2. 4-layer design.
3. Surface-mount parts on top and bottom sides.
4. Material: 0.062" (+/- 0.007") thick glass epoxy FR-4 (green) 1 oz. copper all layers, finished.
5. Finish: Must be lead free. SMOBC (HASL) if available.
6. Hole sizes are finished diameter after plating with 0.0010" minimum plating all surfaces. (Except 20 mil via which MAY be plated closed.) Drilled holes are +/- 0.003" tolerance.
7. Layer-to-layer registration to be +/-0.005"
8. Soldermask all exposed copper, LPI, GREEN color.
9. Silkscreen using epoxy-based ink (white).
10. Surface to be flat within 0.010" in/in of diagonal measurement.
11. Vendor shall etch, silkscreen or stamp I.D. logo and date code, type designation and UL flame rating on top side of PCB. NO COPPER MAY BE DELETED
12. Soldercoat both sides to standard J-STD-003.
13. Finished pcb shall have 0.0035" min dielectric material between consecutive conductor layers when cured.
14. Mechanical dims are +/- 0.005" tolerance.
15. Workmanship and acceptance criteria shall be in accordance with IPC-A-600, Class 1.



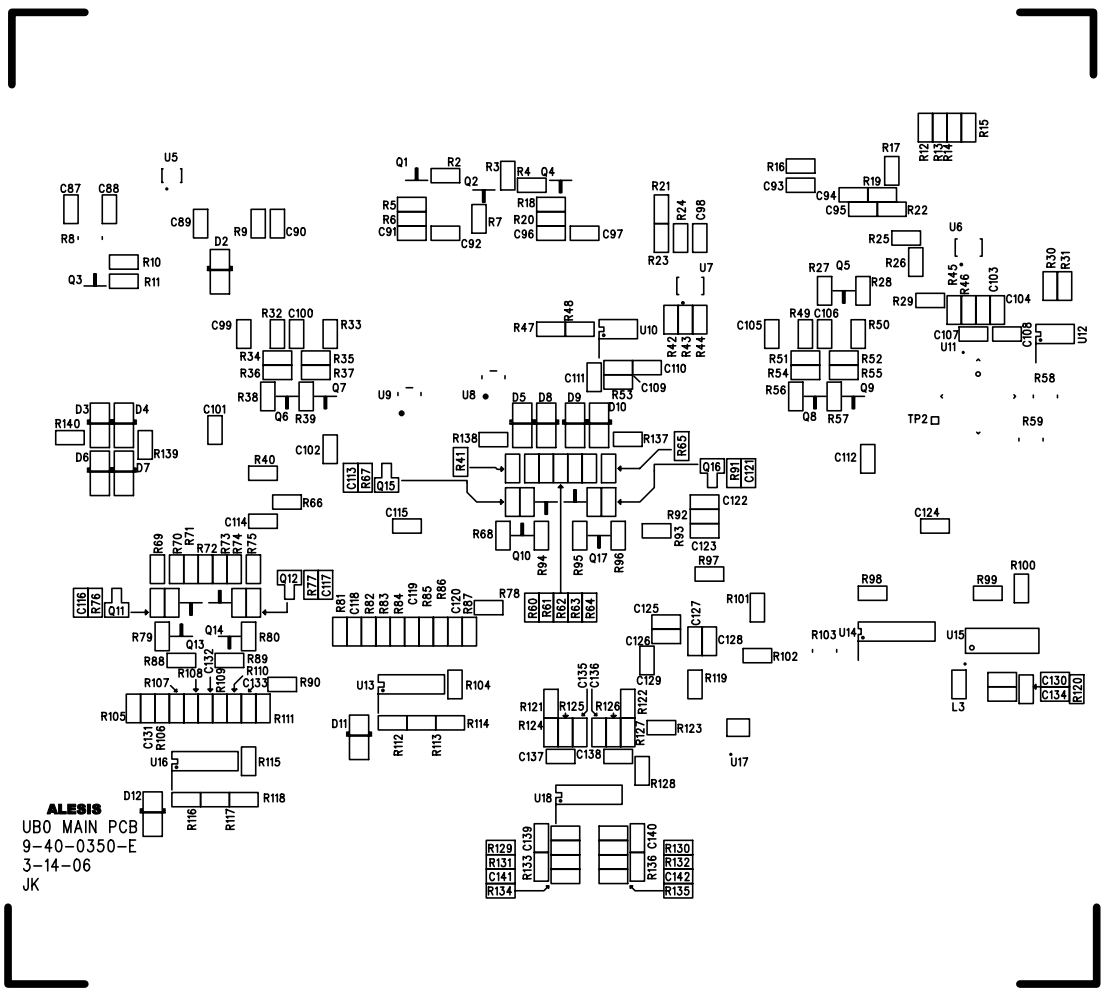
ALESIS 9-40-0350-E "PWRPLANE LAYER 3"



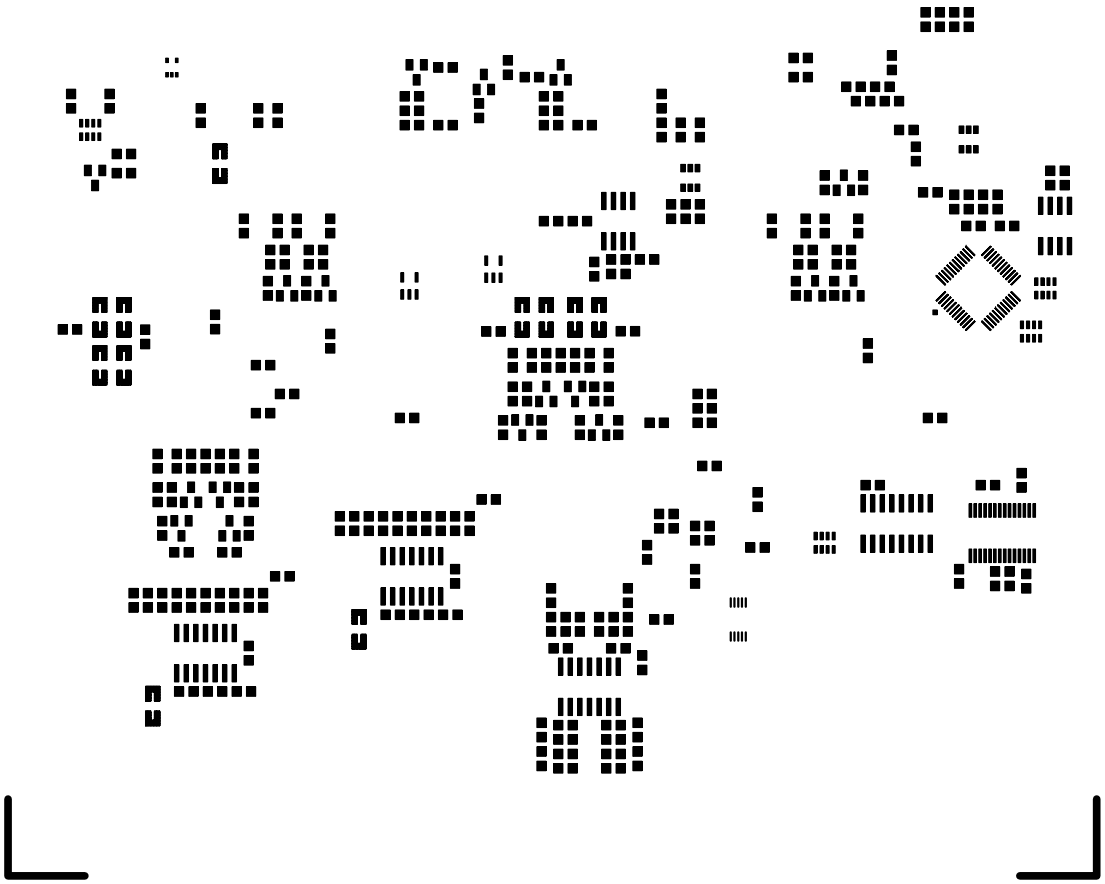
ALESIS 9-40-0350-E "BOTTRACE"



ALESIS 9-40-0350-E "BOTSMK"

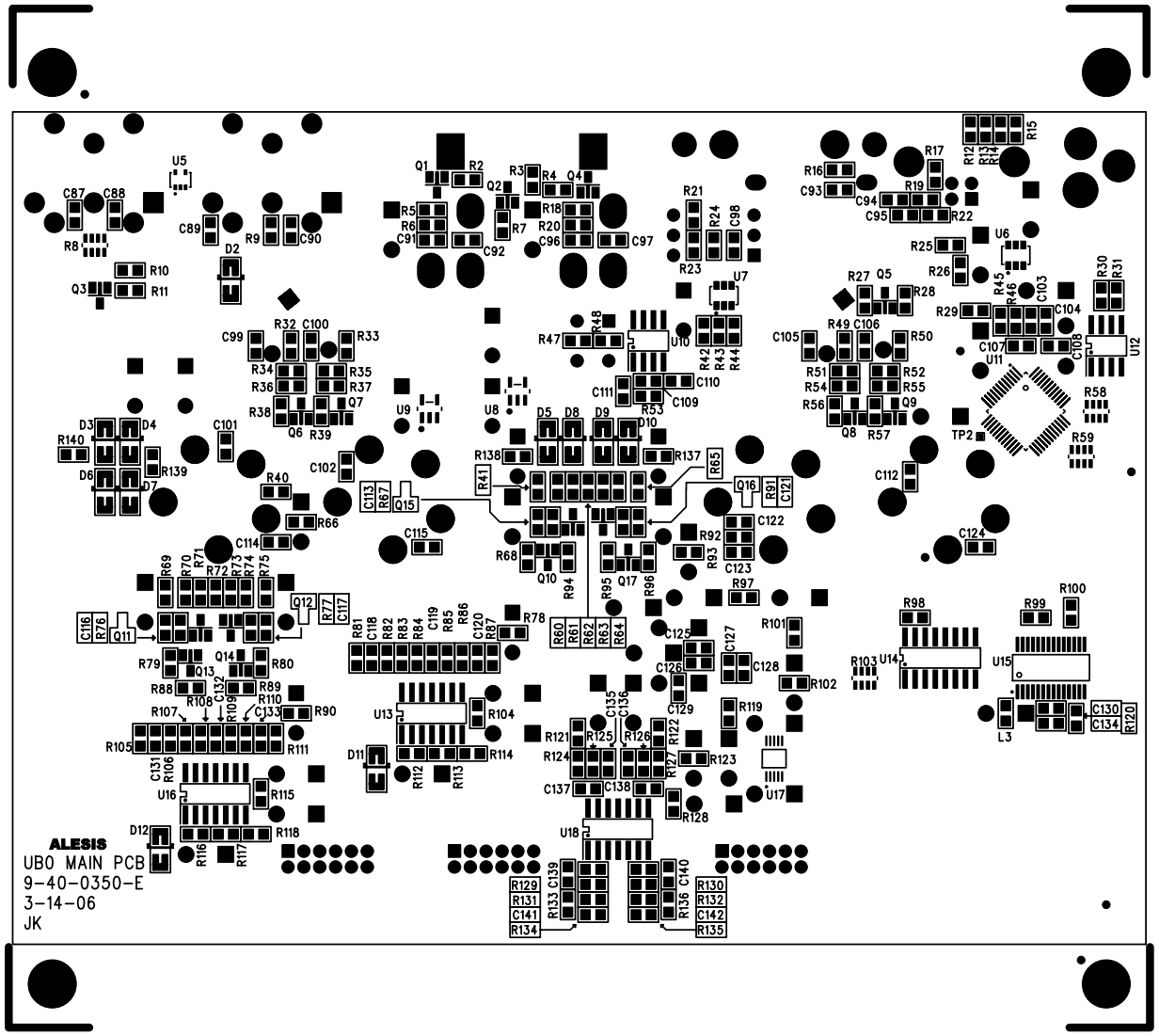


ALESIS 9-40-0350-E "BOTSILK"



ALESIS 9-40-0350-E "BOTPASTE"

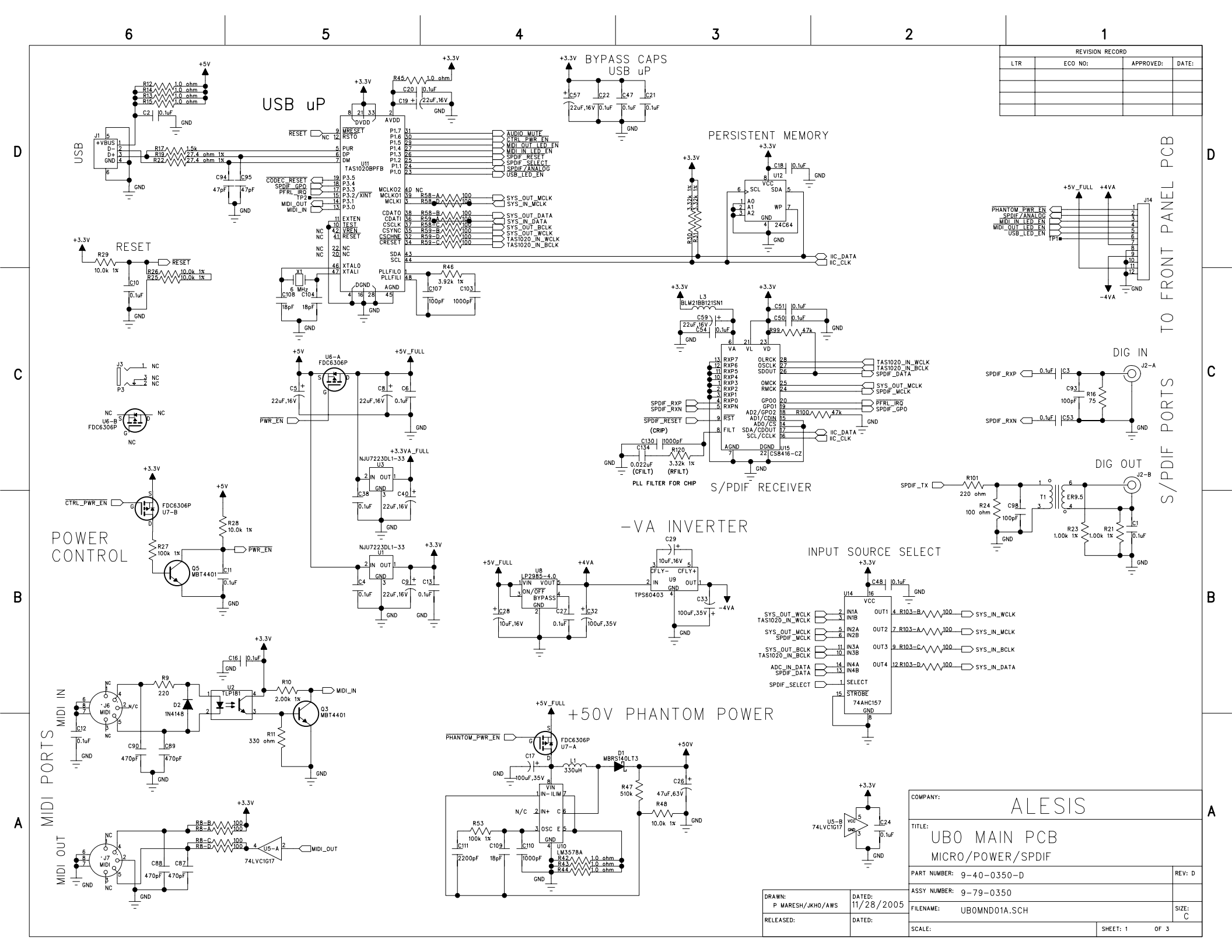
ALESIS 9-79-0350-E "BOTTOM ASSEMBLY DRAWING"

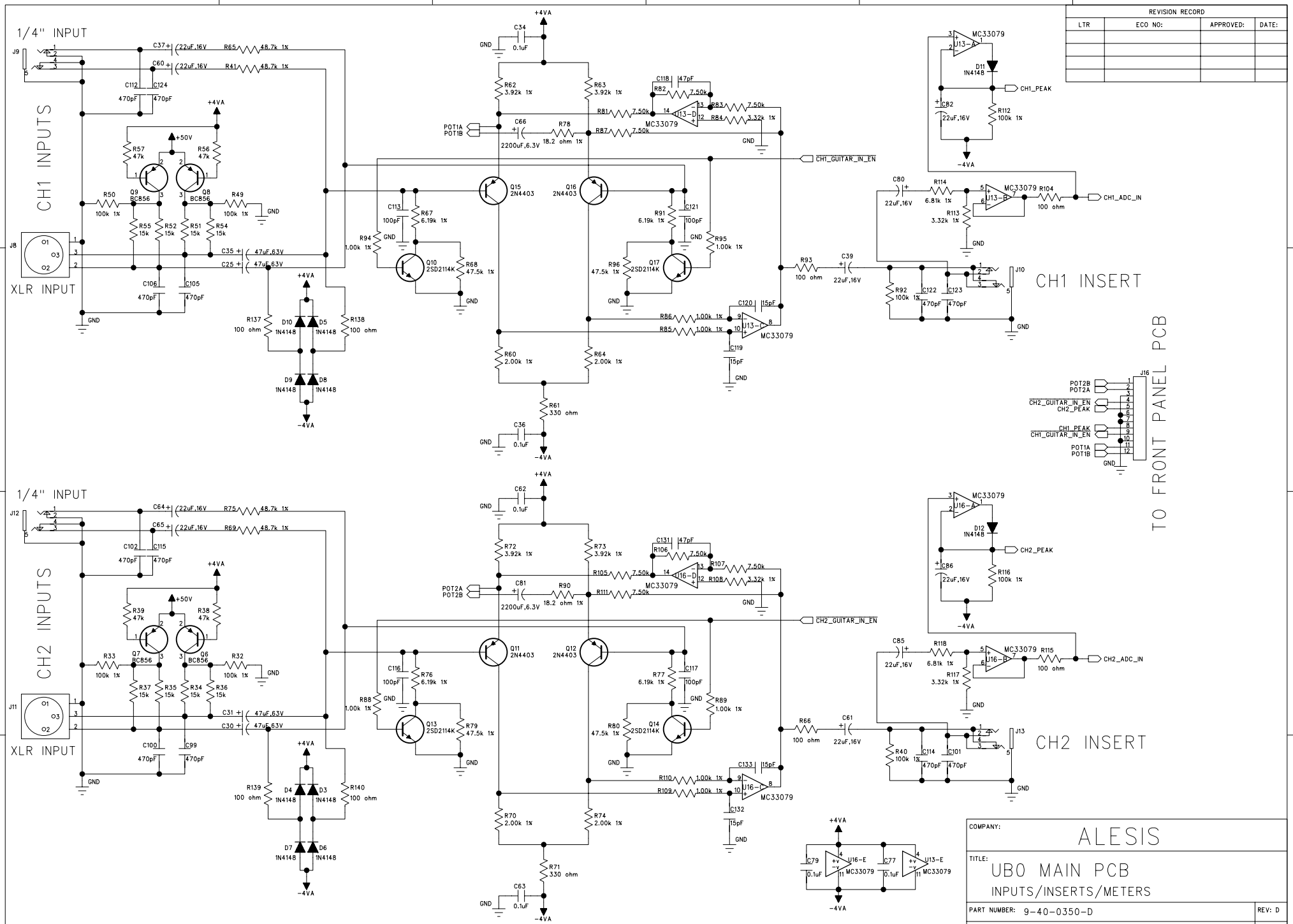


	UB0MNE - Main PCB Rev E						**Last Revised:**	
	RevChange Document						**3/13/2006**	
SCH	**PCB**	**CAM**	**Suggested by:**	**DATE**	**Performed by:**	**DATE**	**Description of change:**	**Reason for change:**
							TOP LEVEL CHANGES	
x	x		SOP	12/2/2005	JK	3/13/2006	Change all text from Rev D to E	SOP
x	x		SOP	12/2/2005	JK	3/13/2006	update all Part Types	SOP
			SOP	12/2/2005			Review/Integrate all outstanding ECNs	SOP
							Note: ***A new solderpaste stencil IS NOT required***	No components were changed or moved.
x	x		JK	3/10/2006	JK	3/13/2006	Correct implementation of input protection diodes and 100 - Ohm series resistors.	The current implementation does not provide much protection, if any at all.
							SCHEMATIC CHANGES	
							PCB CHANGES	

MAIN PCB

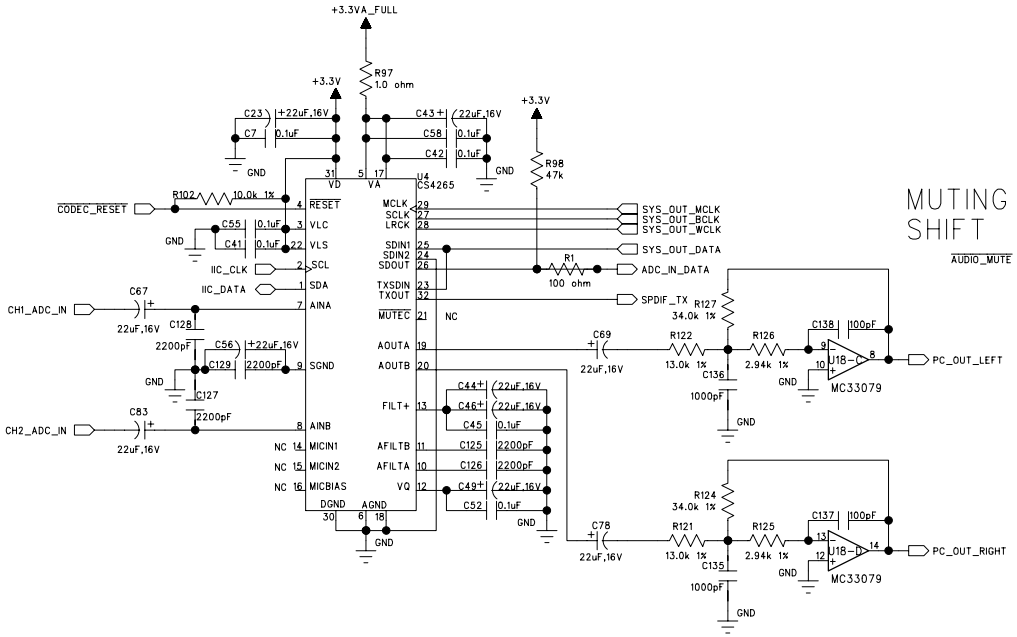
REV D


REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
USB uP
BYPASS CAPS
USB uP
PERSISTENT MEMORY
RESET
TO FRONT PANEL PCB
S/PDIF PORTS
DIG IN
DIG OUT
S/PDIF RECEIVER
PLL FILTER FOR CHIP
POWER CONTROL
-VA INVERTER
INPUT SOURCE SELECT
MIDI PORTS
MIDI IN
MIDI OUT
+50V PHANTOM POWER
COMPANY:
ALESIS
TITLE:
UB0 MAIN PCB
MICRO/POWER/SPDIF
PART NUMBER: 9-40-0350-D
REV: D
ASSY NUMBER: 9-79-0350
FILENAME: UB0MND01A.SCH
SIZE: C
SCALE:
SHEET: 1 OF 3
DRAWN: P MARESH/JKHO/AWS
DATED: 11/28/2005
RELEASED:
DATED:

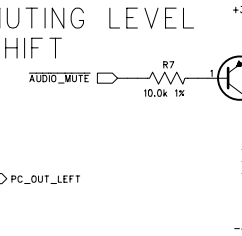

1/4" INPUT
CH1 INPUTS
XLR INPUT
CH1_GUITAR_IN_EN
CH1_PEAK
CH1_ADC_IN
CH1 INSERT
TO FRONT PANEL PCB
1/4" INPUT
CH2 INPUTS
XLR INPUT
CH2_GUITAR_IN_EN
CH2_PEAK
CH2_ADC_IN
CH2 INSERT
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
COMPANY:
ALESIS
TITLE:
UBO MAIN PCB
INPUTS/INSERTS/METERS
PART NUMBER: 9-40-0350-D
REV: D
ASSY NUMBER: 9-79-0350
FILENAME: UBOMND01A.SCH
SIZE: C
SCALE:
SHEET: 2 OF 3
DRAWN: P MARESH/JKHO/AWS
DATED: 11/28/2005
RELEASED:
DATED:

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

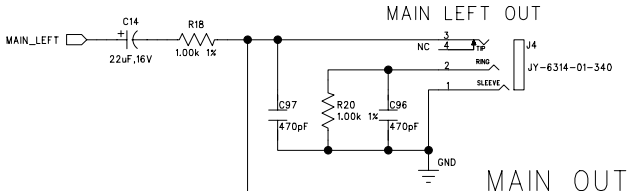
SPDIF OUT
CH1/2 IN ADC, PC OUT DAC



MUTING LEVEL SHIFT

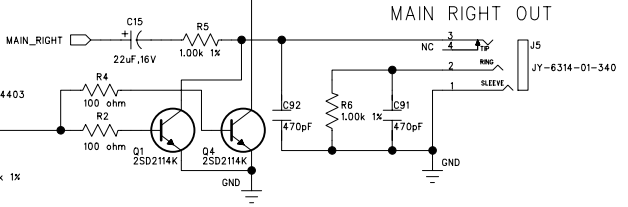


MAIN LEFT OUT

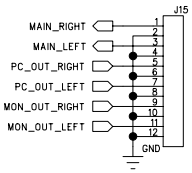


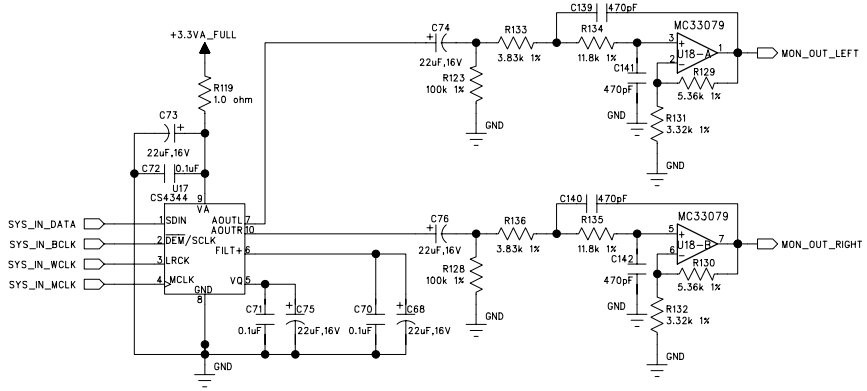
MAIN OUTS

MAIN RIGHT OUT

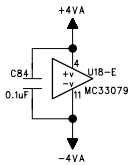


TO FRONT PANEL PCB



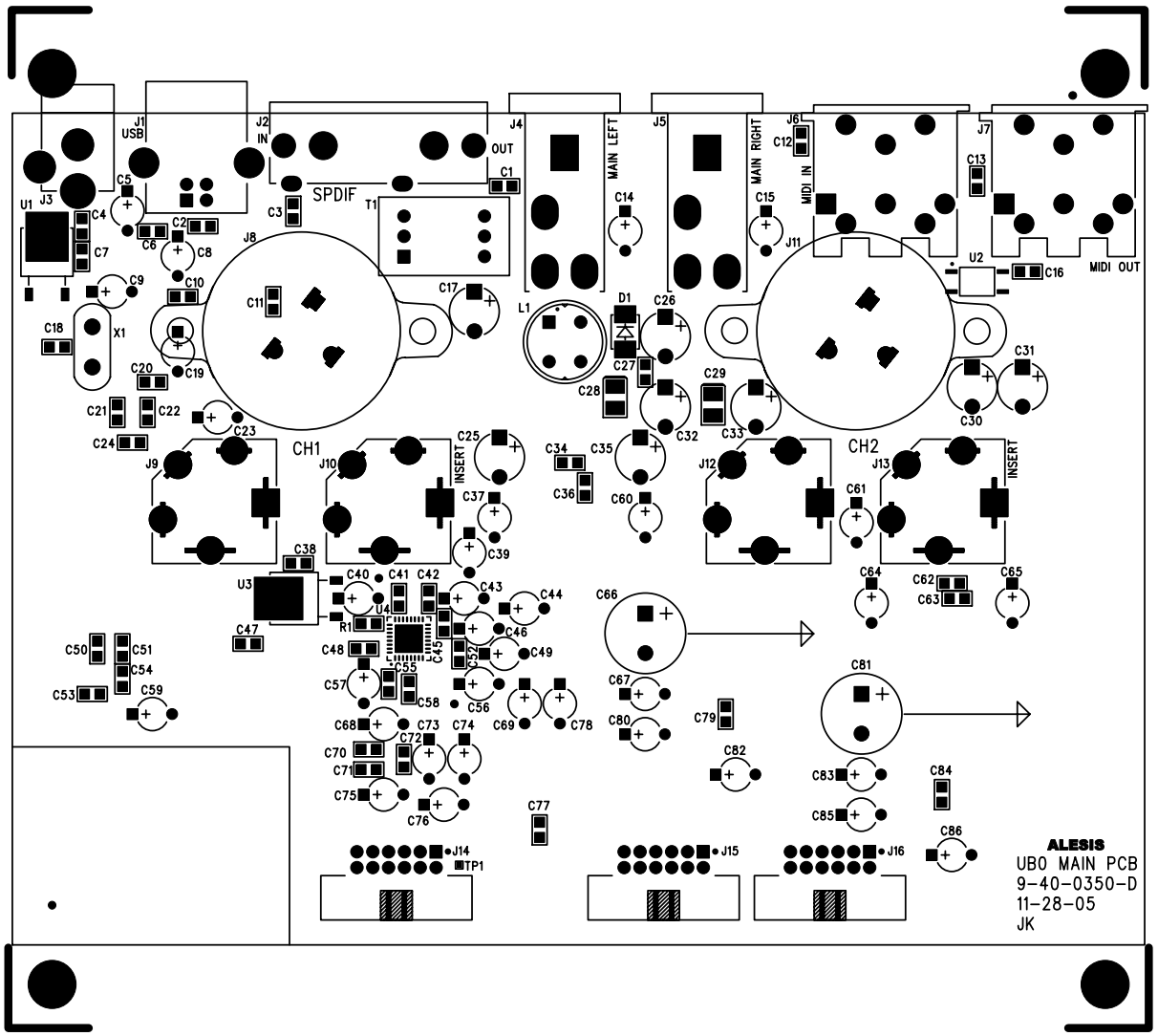


MONITOR DAC



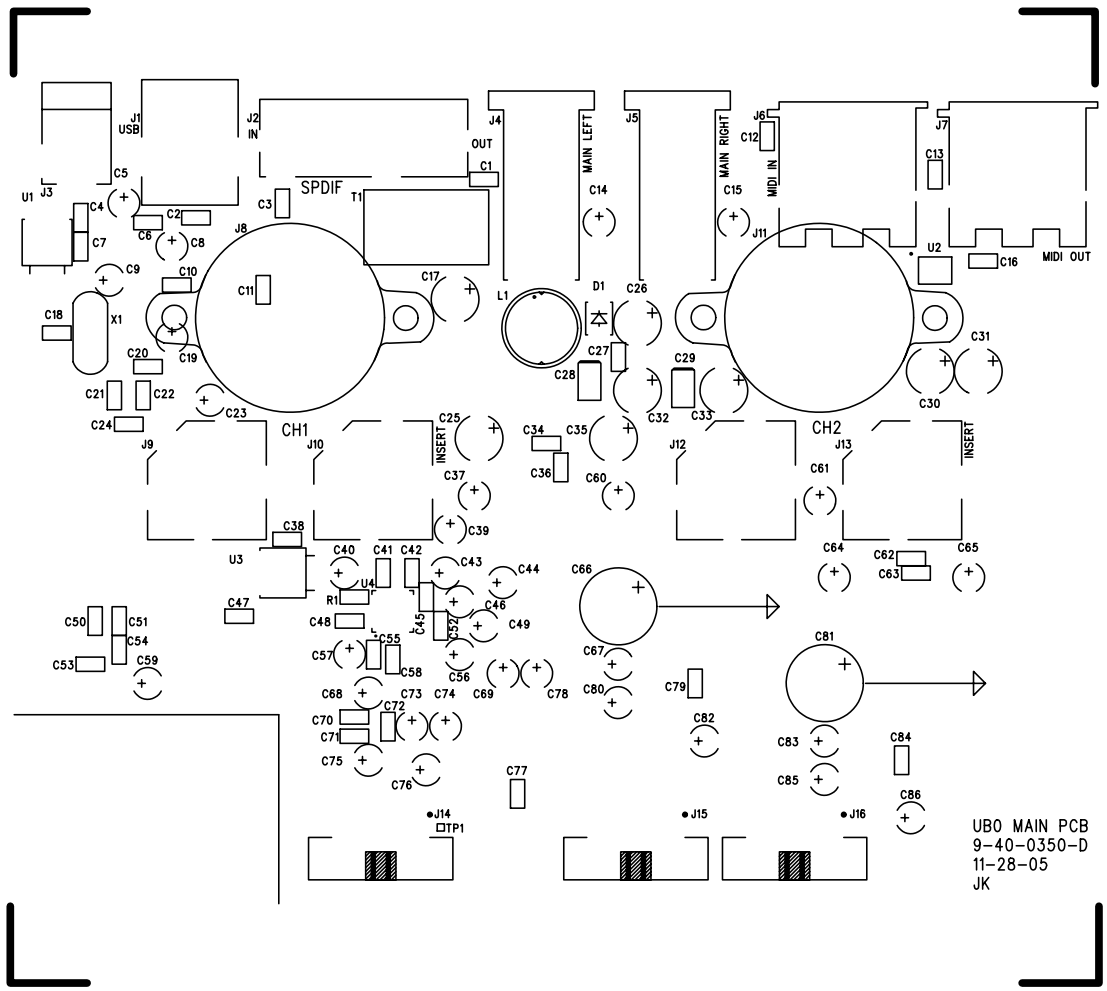
DRAWN: P MARESH/JKHO/AWS	DATED: 11/28/2005	COMPANY: ALESIS	
RELEASED:	DATED:	TITLE: UBO MAIN PCB OUTPUTS/CONVERTERS	
		PART NUMBER: 9-40-0350-D	REV: D
		ASSY NUMBER: 9-79-0350	
		FILENAME: UBOMND01A.SCH	SIZE: C
		SCALE:	SHEET: 3 OF 3

ALESIS 9-79-0350-D "TOP ASSEMBLY DRAWING"

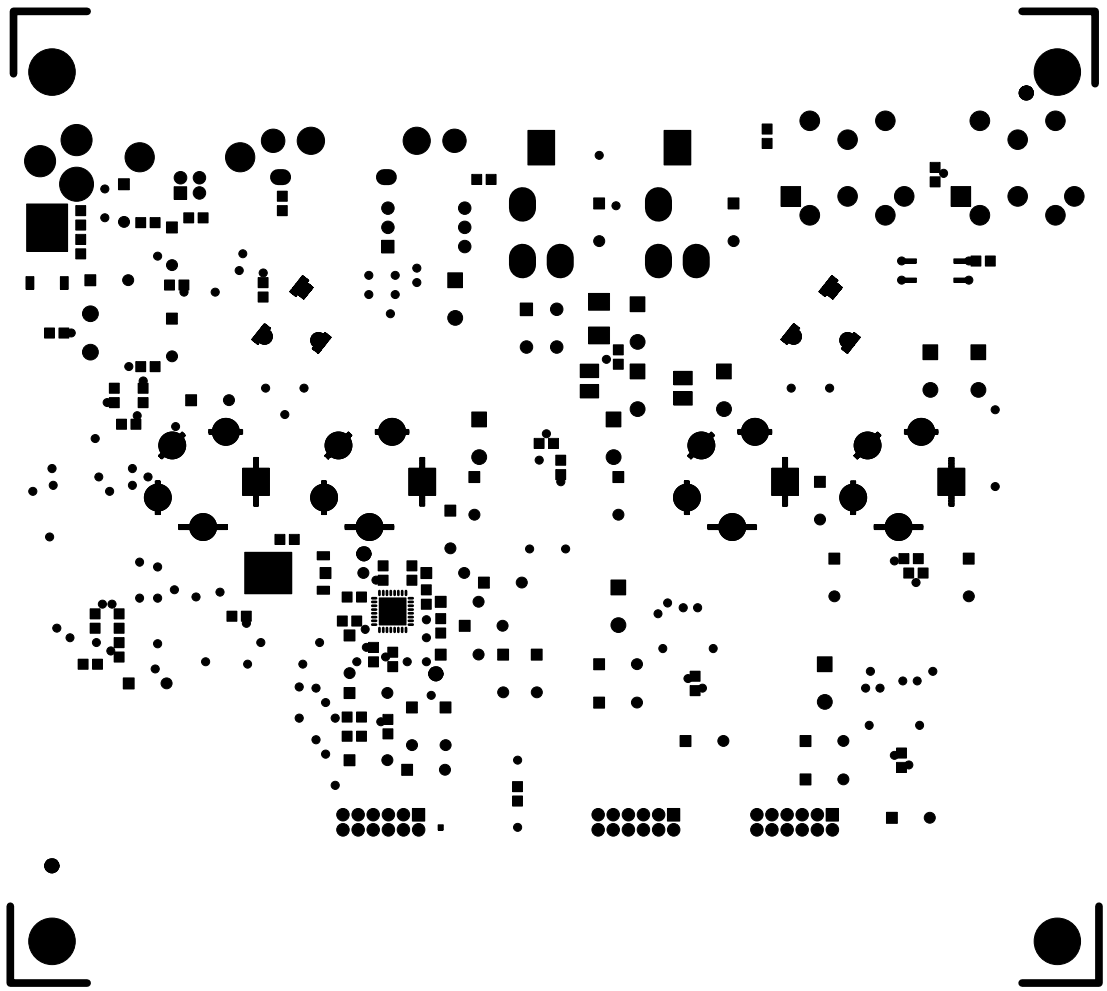




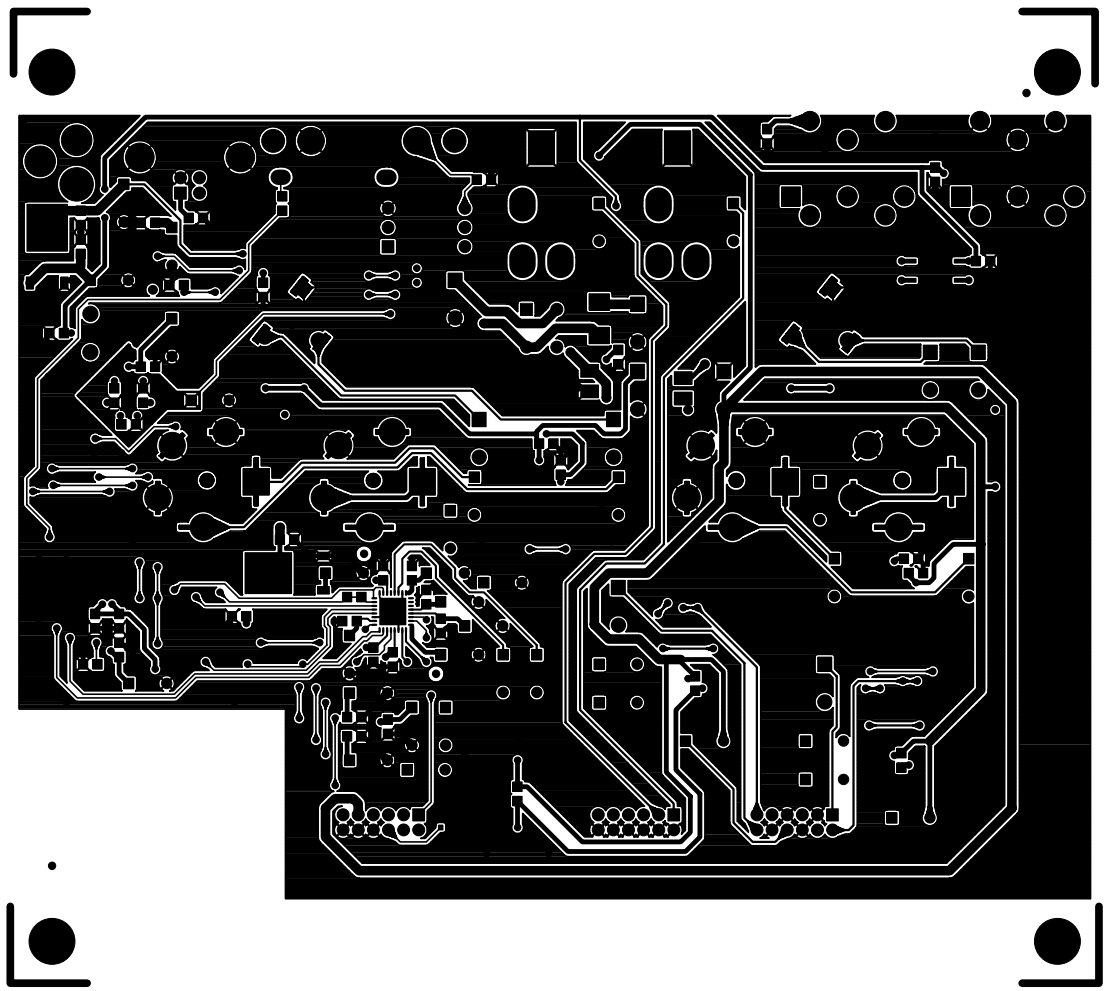
ALESIS 9-40-0350-D"TOPPASTE"



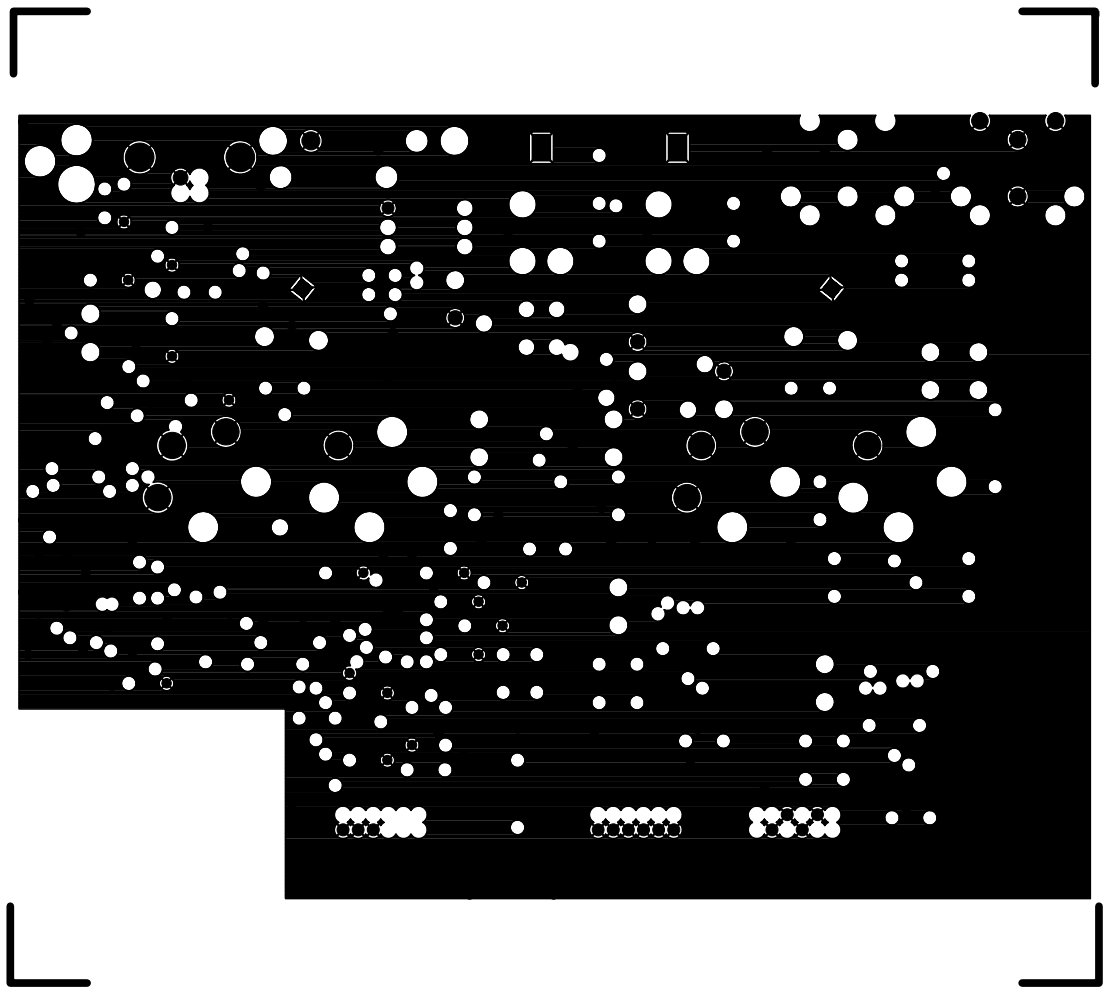
ALESIS 9-40-0350-D "TOPSILK"



ALESIS 9-40-0350-D "TOPSMK"

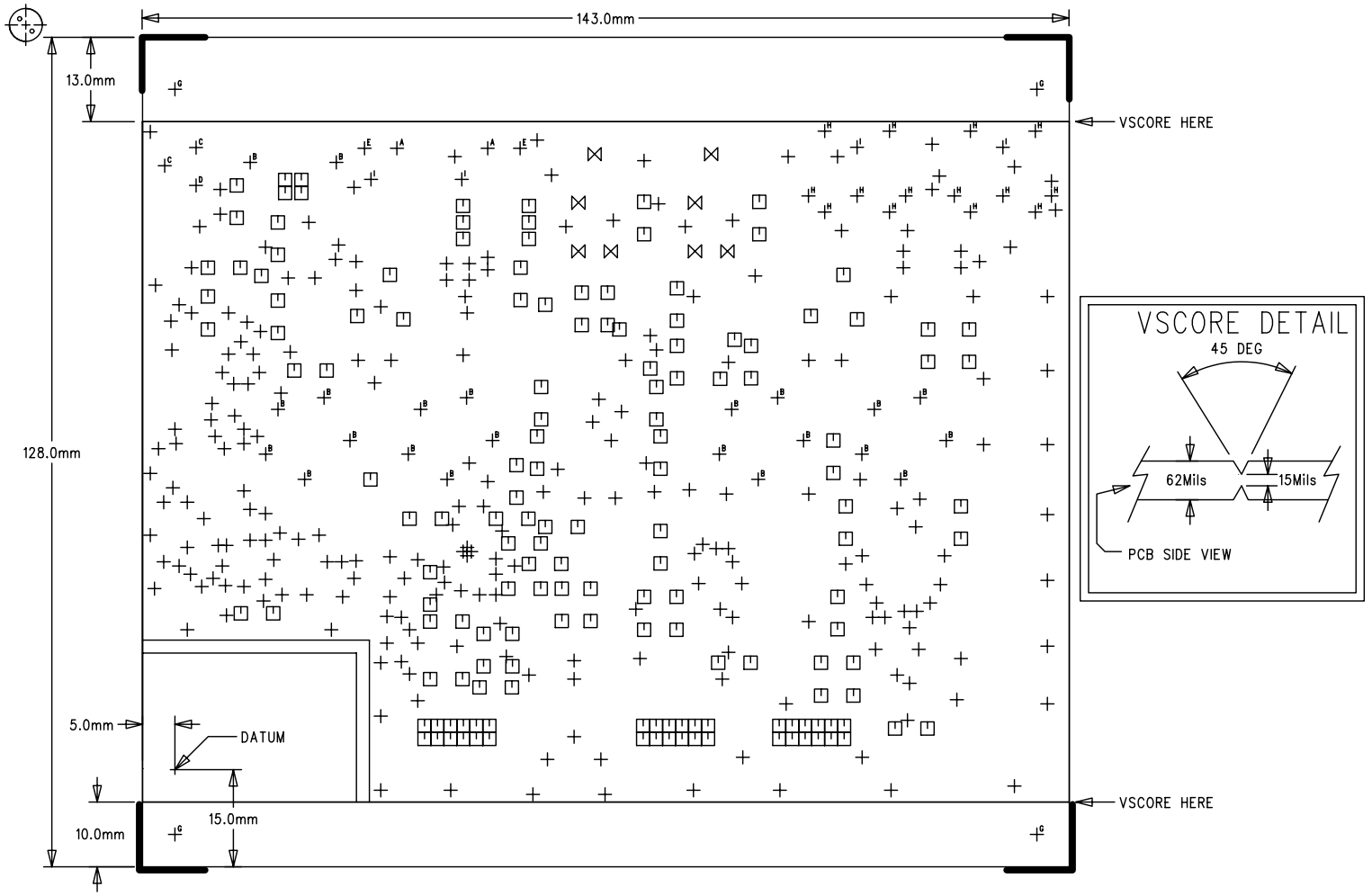


ALESIS 9-40-0350-D "TOPTRACE"



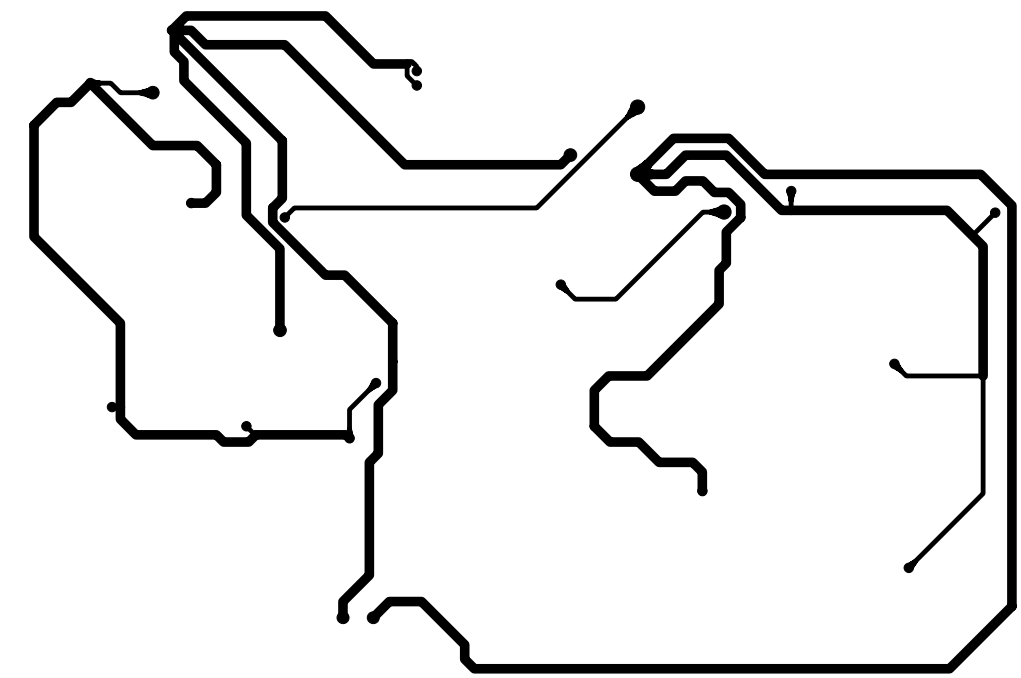
ALESIS 9-40-0350-D "GNDPLANE LAYER 2"

ALESIS 9-40-0350-D "DRILLDWG"

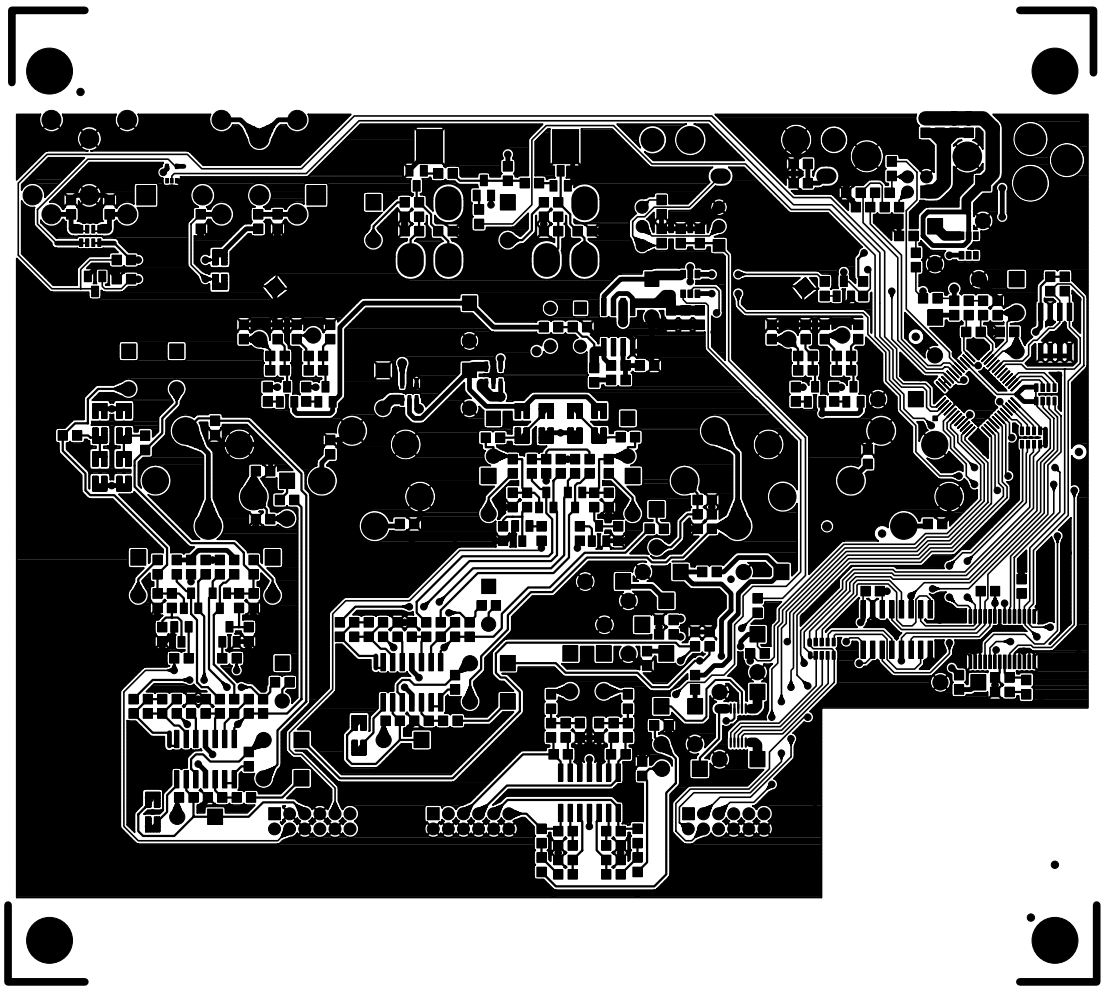


SIZE	QTY	SYM	PLATED	TOL
20	241	+	YES	+/-3
37	153	□	YES	+/-3
82.7	8	⊠	YES	+/-3
86.6	2	A	YES	+/-3
90.6	22	B	YES	+/-3
100.4	2	C	YES	+/-3
125	1	D	YES	+/-3
126	2	E	NO	+/-3
157.5	4	G	NO	+/-0.0
43.3	14	H	YES	+/-0.0
49.2	4	I	YES	+/-0.0

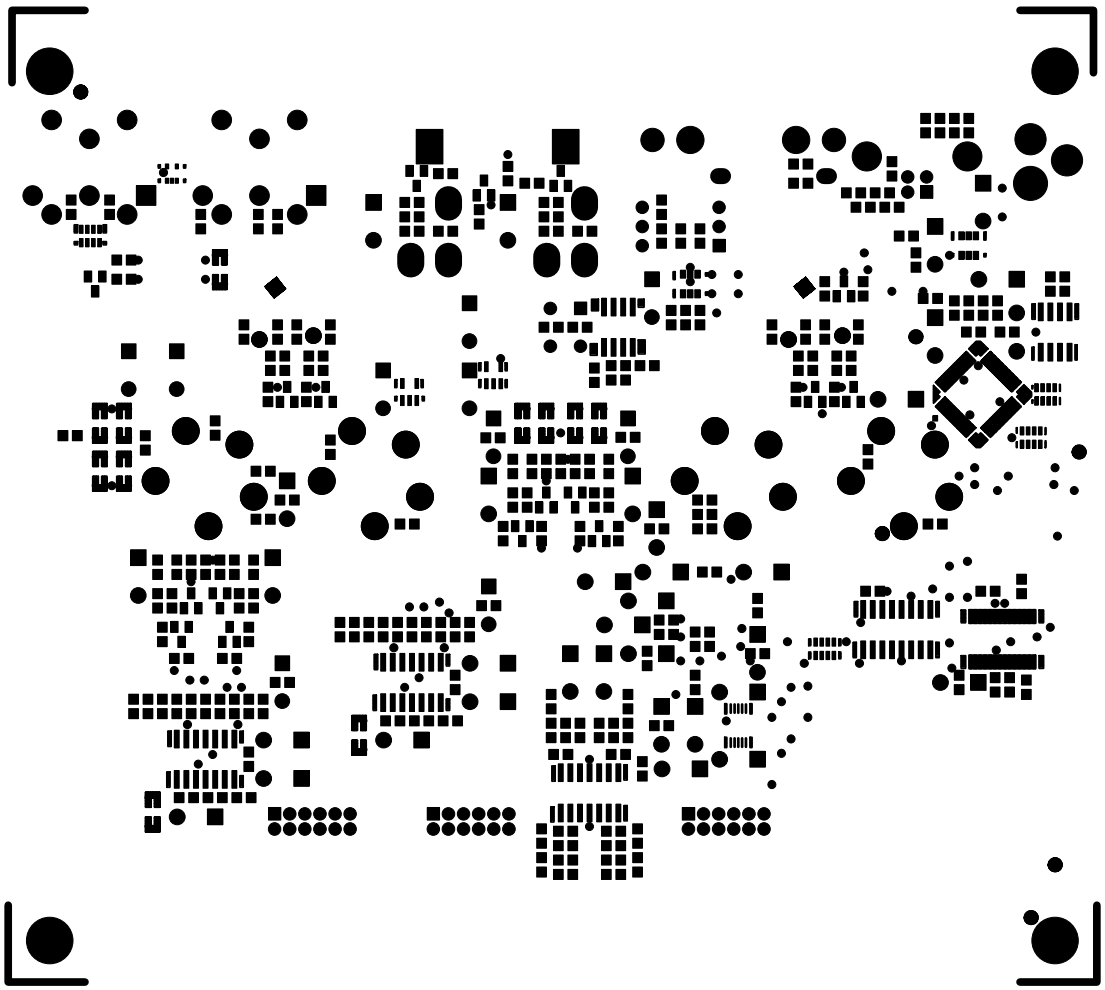
1. Design rules used: 0.008" lines. 0.008" space
2. 4-layer design.
3. Surface-mount parts on top and bottom sides.
4. Material: 0.062" (+/- 0.007") thick glass epoxy FR-4 (green) 1 oz. copper all layers, finished.
5. Finish: SMOBC, Hot Air Level
6. Hole sizes are finished diameter after plating with 0.0010" minimum plating all surfaces. (Except 20 mil via whose finished size is unimportant.) Drilled holes are +/- 0.003" tolerance.
7. Layer-to-layer registration to be +/-0.005"
8. Soldermask all exposed copper, LPI, GREEN color.
9. Silkscreen using epoxy-based ink (white).
10. Surface to be flat within 0.010" in/in of diagonal measurement.
11. Vendor shall etch, silkscreen or stamp I.D. logo and date code, type designation and UL flame rating on top side of PCB. NO COPPER MAY BE DELETED
12. Soldercoat both sides to standard J-STD-003.
13. Finished pcb shall have 0.0035" min dielectric material between consecutive conductor layers when cured.
14. Mechanical dims are +/- 0.005" tolerance.
15. Workmanship and acceptance criteria shall be in accordance with IPC-A-600, Class 1.



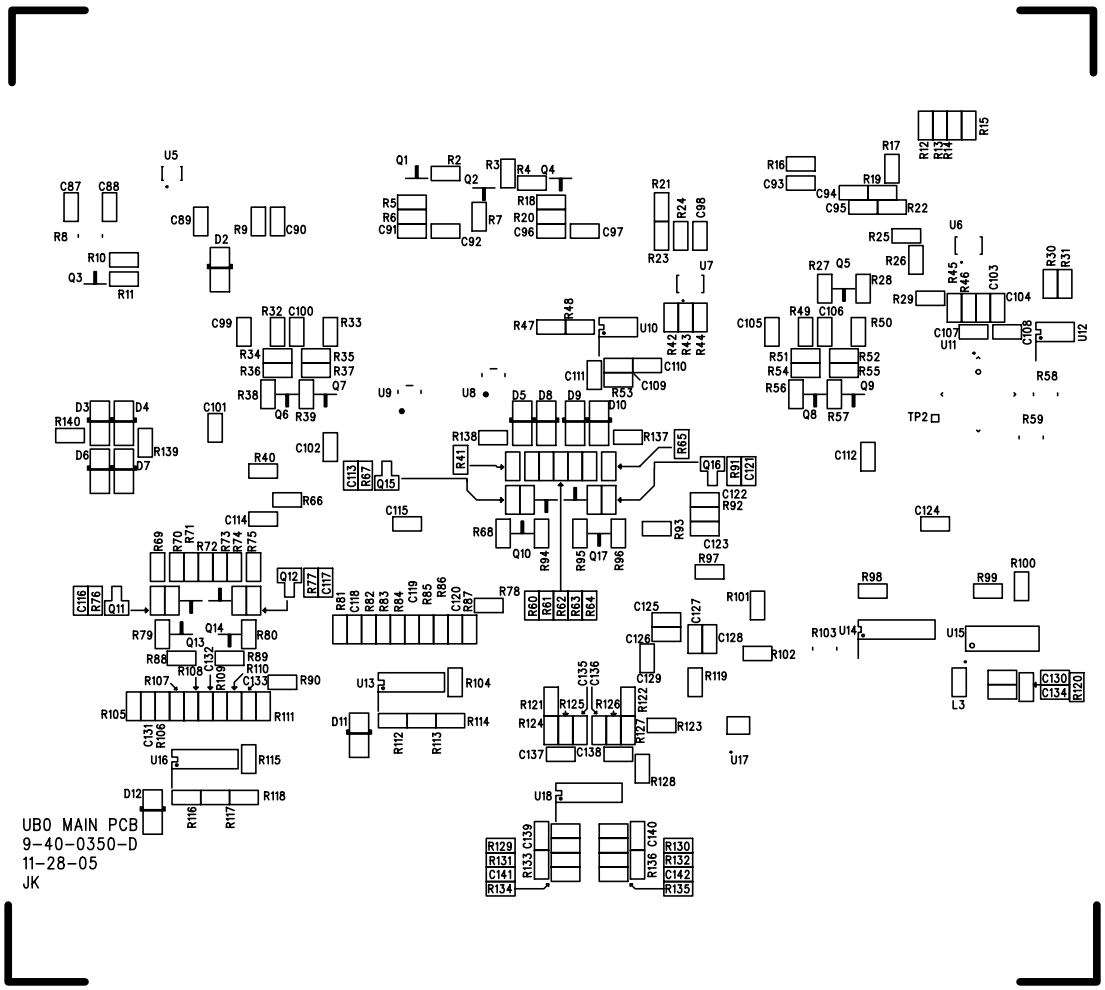
ALESIS 9-40-0350-D "PWRPLANE LAYER 3"



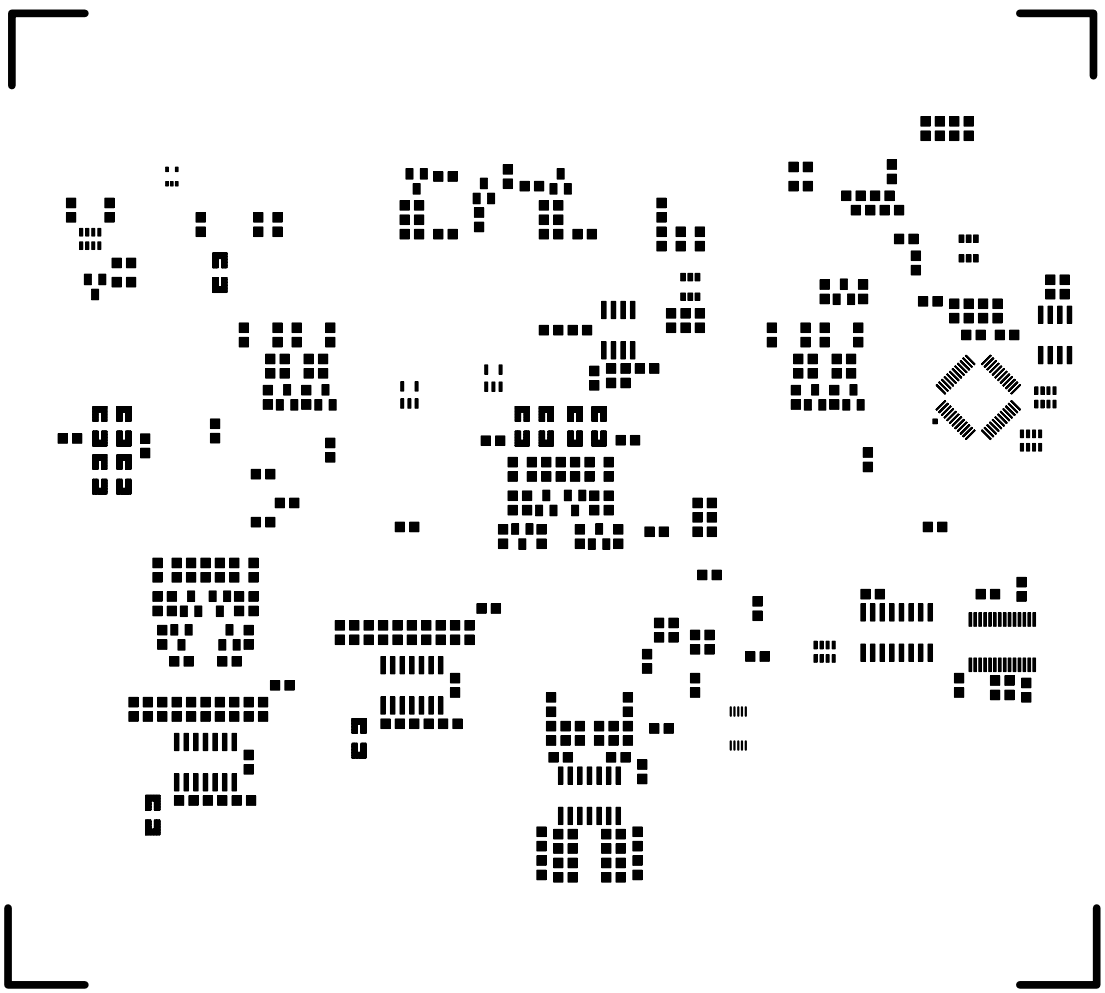
ALESIS 9-40-0350-D "BOTTRACE"



ALESIS 9-40-0350-D "BOTSMK"

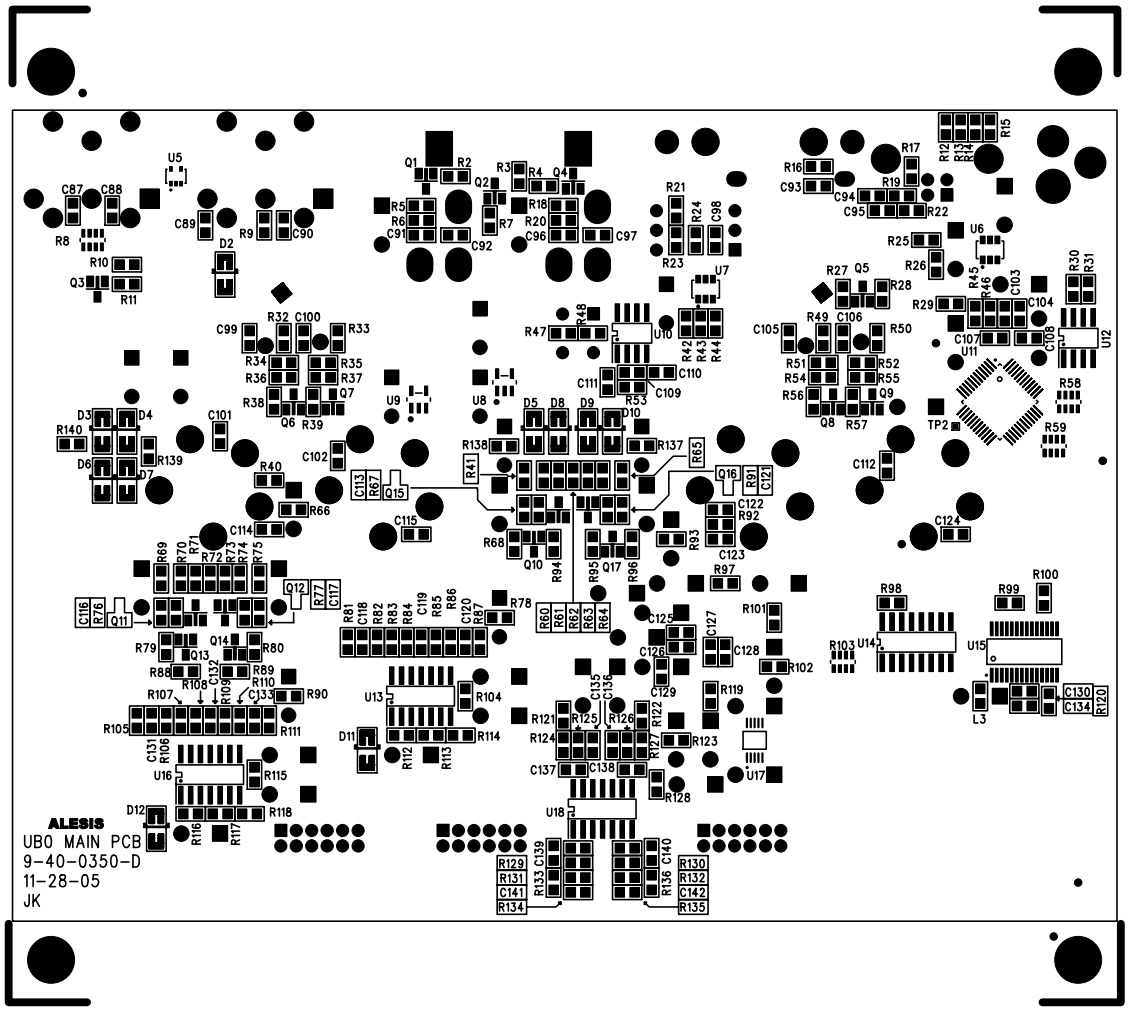


ALESIS 9-40-0350-D "BOTSILK"



ALESIS 9-40-0350-D "BOTPASTE"

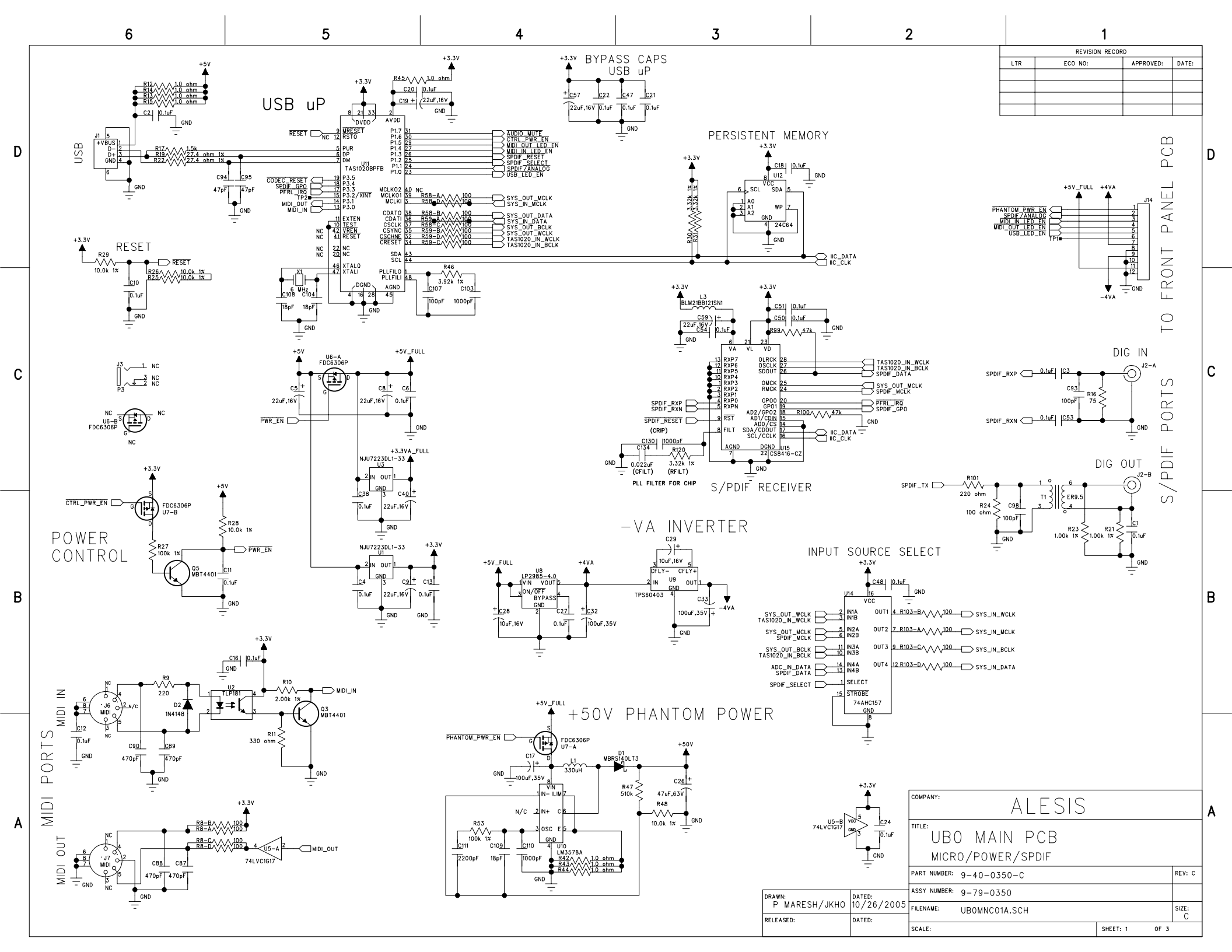
ALESIS 9-79-0350-D "BOTTOM ASSEMBLY DRAWING"

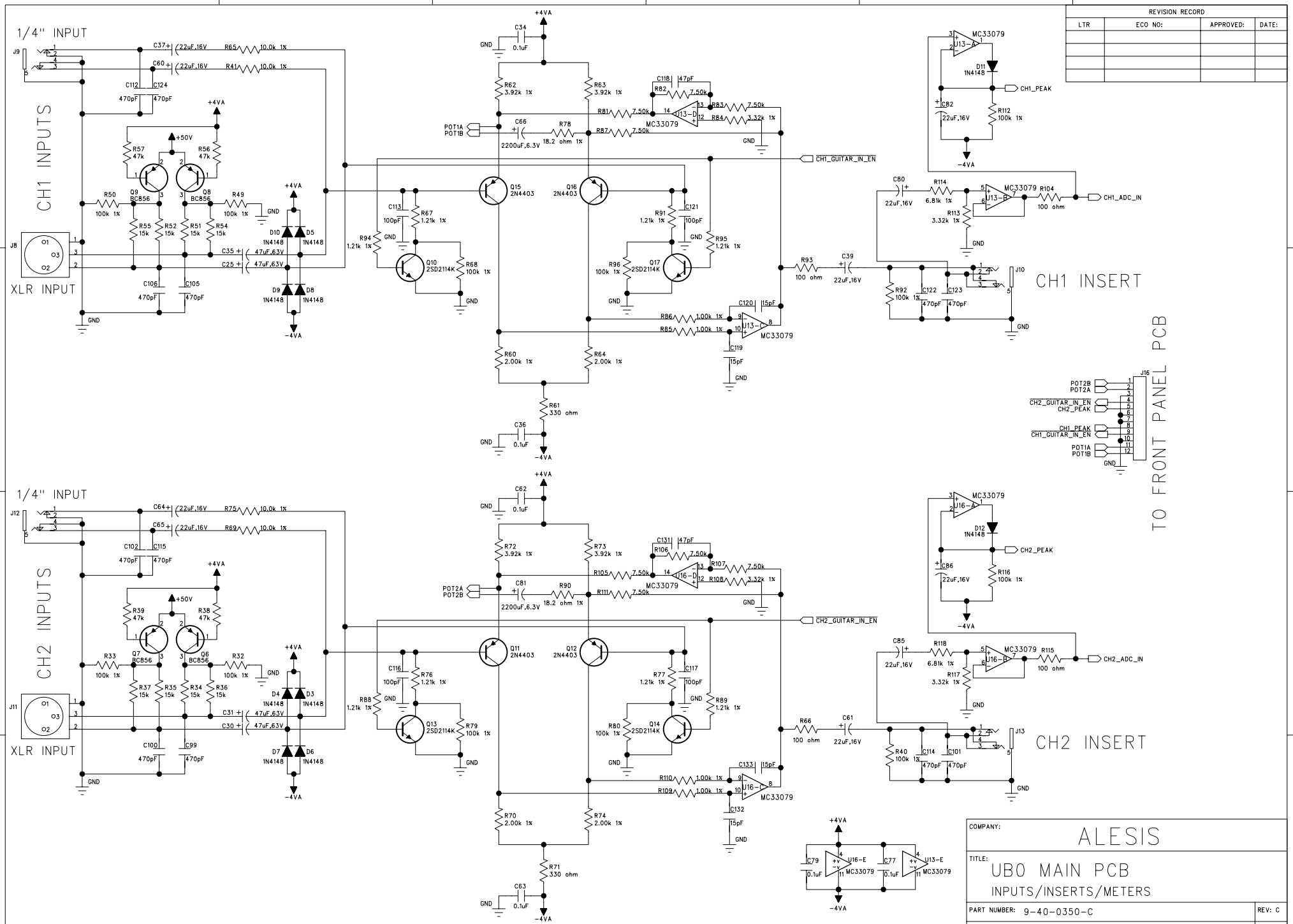


	UB0MND - Main PCB Rev D						**Last Revised:**		
	RevChange Document						**12/1/2005**		
SCH	**PCB**	**CAM**	**Suggested by:**	**DATE**	**Performed by:**	**DATE**	**Description of change:**	**Reason for change:**	
							TOP LEVEL CHANGES		
x	x		SOP	10/26/2005			Change all text from Rev C to #	SOP	
x	x		SOP	10/26/2005			update all Part Types	SOP	
			SOP	10/26/2005			Review/Integrate all outstanding ECNs	SOP	
x	x		MBL	11/16/2005	AWS	12/1/2005	Reduce gain on guitar inputs by 3dB.	Inputs will clip with standard guitar and gain at minimum	
~~x~~	~~x~~		~~MBL~~	~~11/14/2005~~			~~Change headphone volume control to pre-Master volume.~~		This is done on the Front Panel PCB.
x	x		MBL	11/14/2005	AWS	11/29/2005	Add 100ohm resistors between input DC blocking caps (C25, 30, 31, 35) and protection diodes (D3-10).	Protect negative voltage regulator from damage due to short. (This was implemented as rework pre-production so there is no ECN.)	
	x		AWS	11/28/2005	AWS	11/28/2005	Resize holes on MIDI jack footprint. 49.2mil for shield pin, 43.3 mil for other pins	Yahourng request	
	x		AWS	11/28/2005	AWS	11/28/2005	Resize holes on XLR jack footprint	Yahourng request	
	x		AWS	11/28/2005	AWS	11/28/2005	Modify 10mm PEB (PCB?) board edge to 13mm	Yahourng request	
	x		AWS	11/28/2005	AWS	11/28/2005	Modify footprint of 1-08-0222 for 1mm hole size	Yahourng request	
	x		AWS	11/28/2005	AWS	11/28/2005	Unplate corner mounting holes on main pcb	Yahourng request	
							Note: ***A new solderpaste stencil IS required***	Components were added.	
							SCHEMATIC CHANGES		
							PCB CHANGES		

MAIN PCB

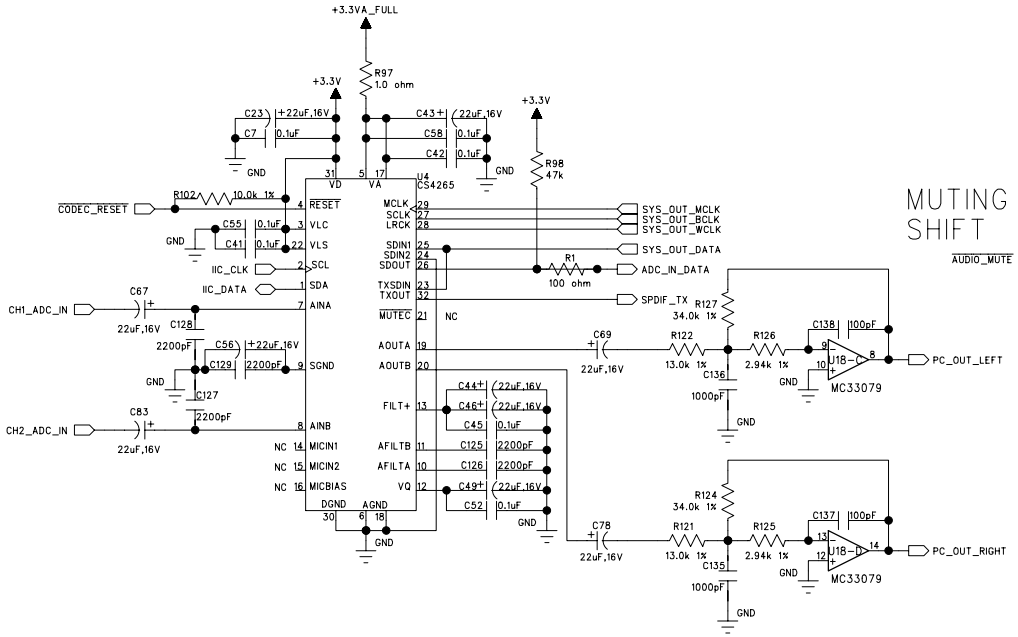
REV C


REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
USB uP
BYPASS CAPS
USB uP
PERSISTENT MEMORY
RESET
USB
TO FRONT PANEL PCB
DIG IN
DIG OUT
S/PDIF PORTS
S/PDIF RECEIVER
PLL FILTER FOR CHIP
POWER CONTROL
-VA INVERTER
INPUT SOURCE SELECT
MIDI PORTS
MIDI IN
MIDI OUT
+50V PHANTOM POWER
ALESIS
UBO MAIN PCB
MICRO/POWER/SPDIF
COMPANY:
TITLE:
PART NUMBER: 9-40-0350-C
REV: C
ASSY NUMBER: 9-79-0350
FILENAME: UBOMNC01A.SCH
SIZE: C
SCALE:
SHEET: 1 OF 3
DRAWN: P MARESH/JKHO
DATED: 10/26/2005
RELEASED:
DATED:

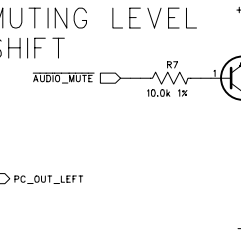

1/4" INPUT
CH1 INPUTS
XLR INPUT
CH1_GUITAR_IN_EN
CH1_PEAK
CH1_ADC_IN
CH1 INSERT
1/4" INPUT
CH2 INPUTS
XLR INPUT
CH2_GUITAR_IN_EN
CH2_PEAK
CH2_ADC_IN
CH2 INSERT
TO FRONT PANEL PCB
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
COMPANY:
ALESIS
TITLE:
UBO MAIN PCB
INPUTS/INSERTS/METERS
PART NUMBER: 9-40-0350-C
REV: C
ASSY NUMBER: 9-79-0350
FILENAME: UBOMNC01A.SCH
SIZE: C
SCALE:
SHEET: 2 OF 3
DRAWN: P MARESH/JKHO
DATED: 10/26/2005
RELEASED:
DATED:

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

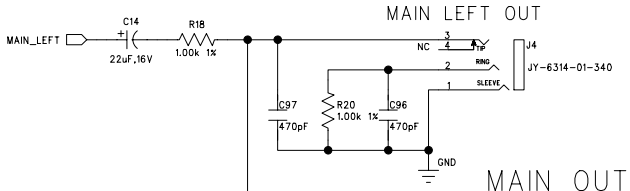
SPDIF OUT
CH1/2 IN ADC, PC OUT DAC



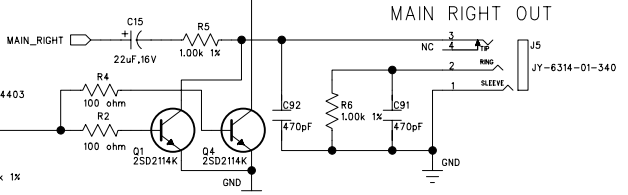
MUTING LEVEL SHIFT



MAIN LEFT OUT

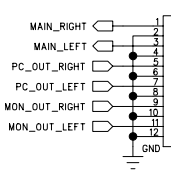


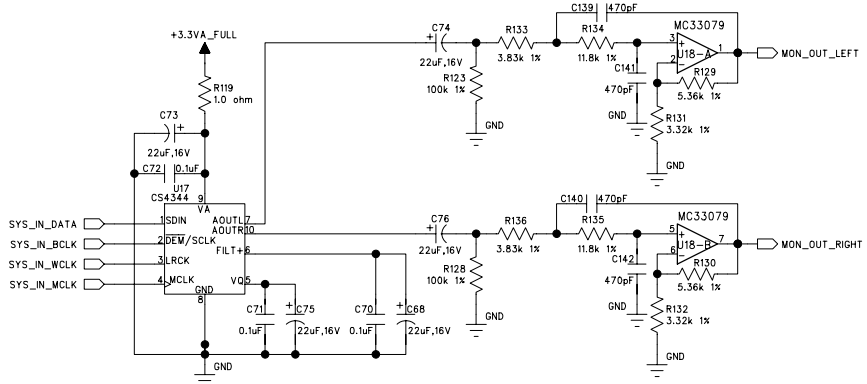
MAIN RIGHT OUT



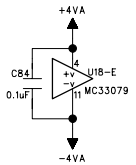
MAIN OUTS

TO FRONT PANEL PCB



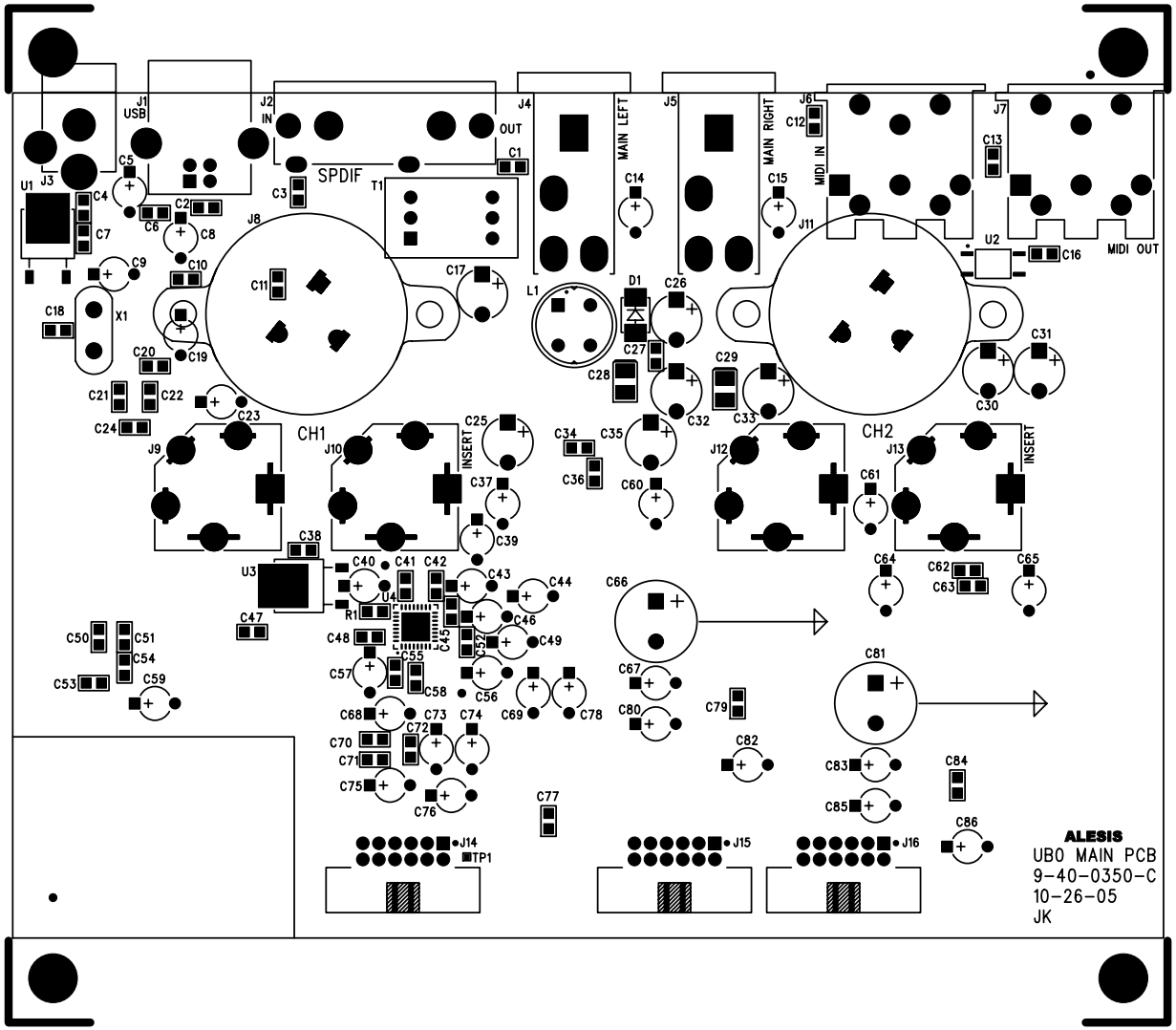


MONITOR DAC



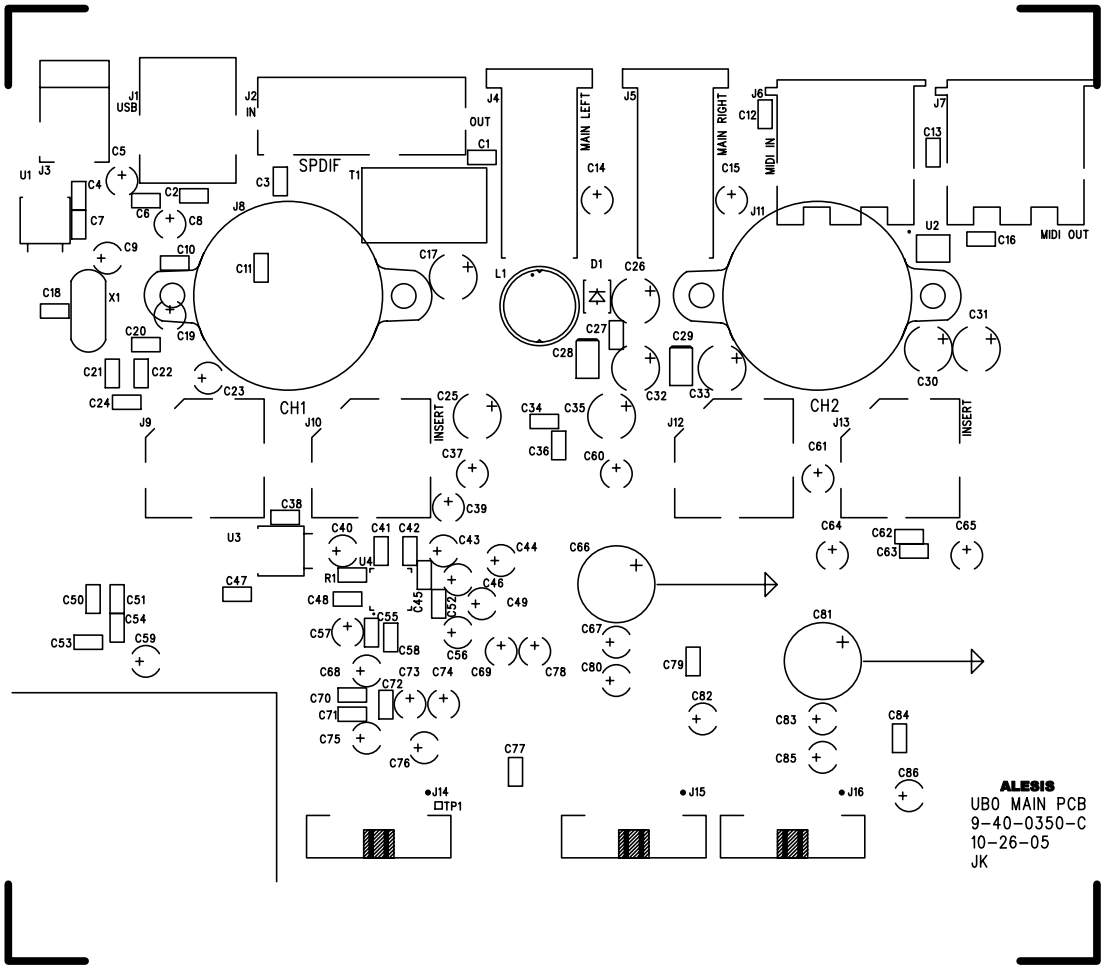
DRAWN: P MARESH/JKHO	DATED: 10/26/2005	COMPANY: ALESIS	
RELEASED:	DATED:	TITLE: UBO MAIN PCB OUTPUTS/CONVERTERS	
		PART NUMBER: 9-40-0350-C	REV: C
		ASSY NUMBER: 9-79-0350	
		FILENAME: UBOMNC01A.SCH	SIZE: C
		SCALE:	SHEET: 3 OF 3

ALESIS 9-79-0350-C "TOP ASSEMBLY DRAWING"

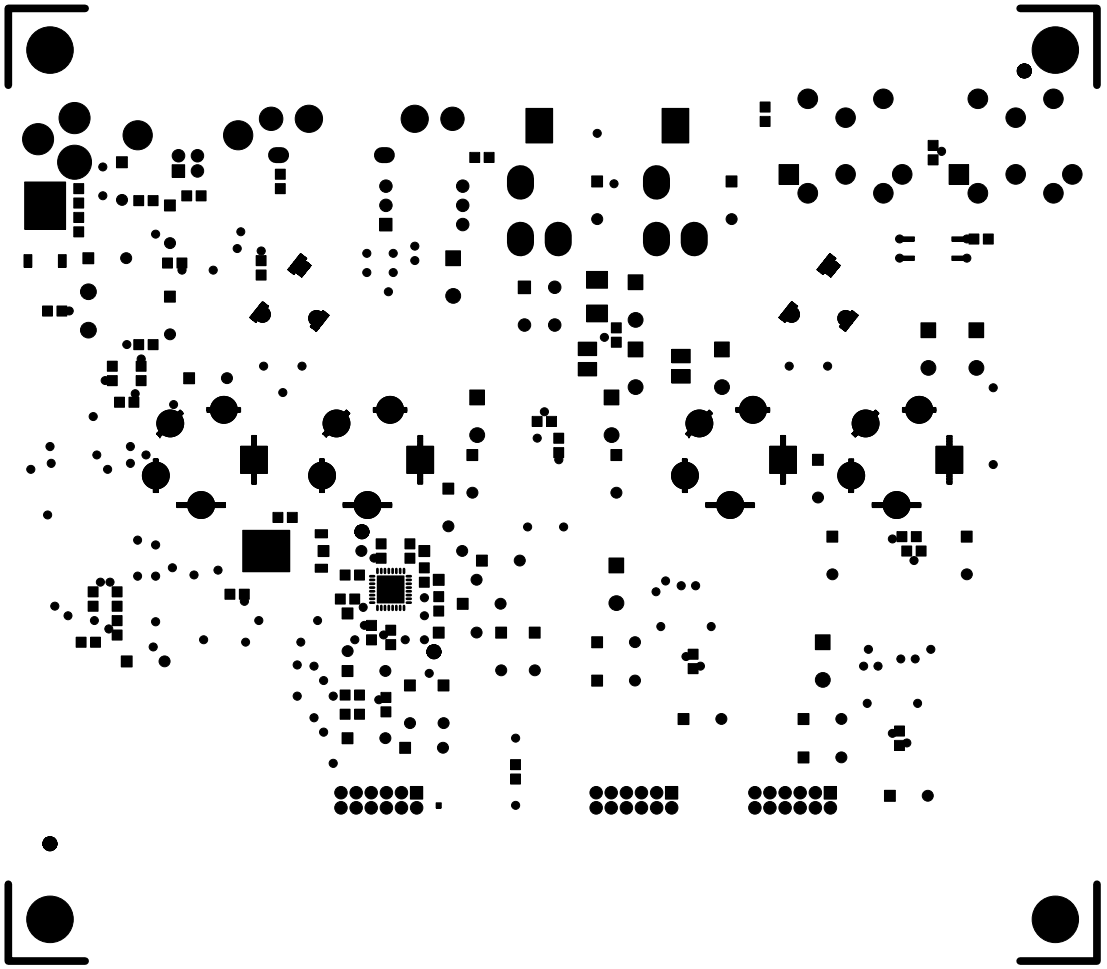




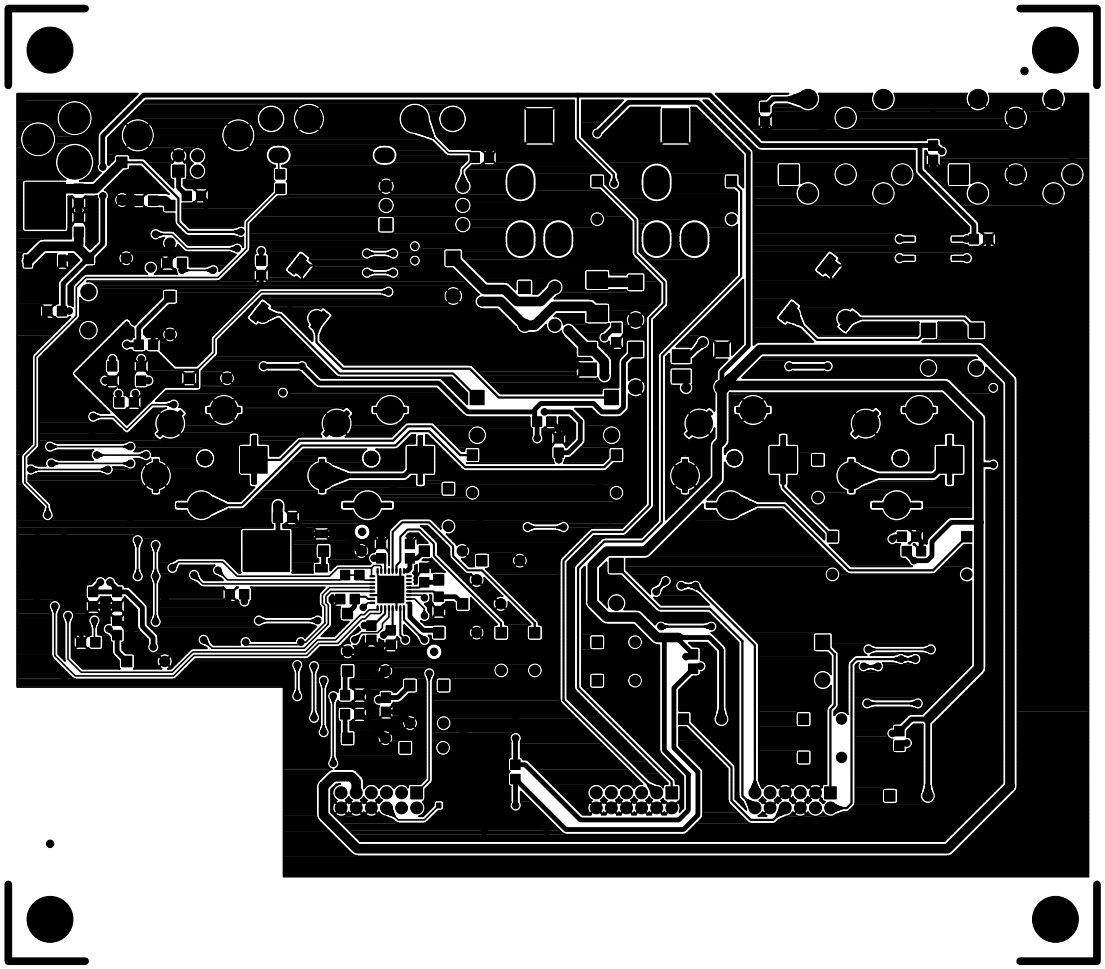
ALESIS 9-40-0350-C"TOPPASTE"



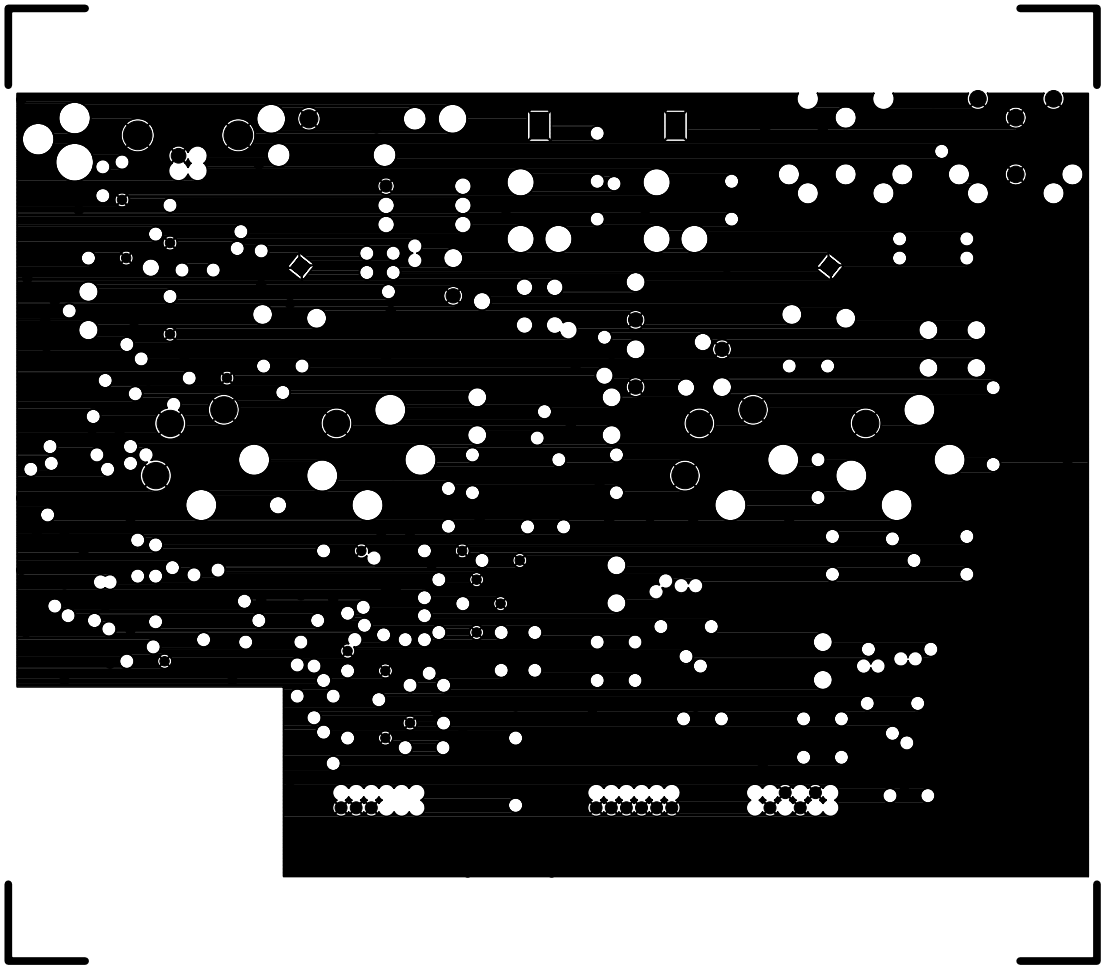
ALESIS 9-40-0350-C "TOPSILK"



ALESIS 9-40-0350-C "TOPSMK"

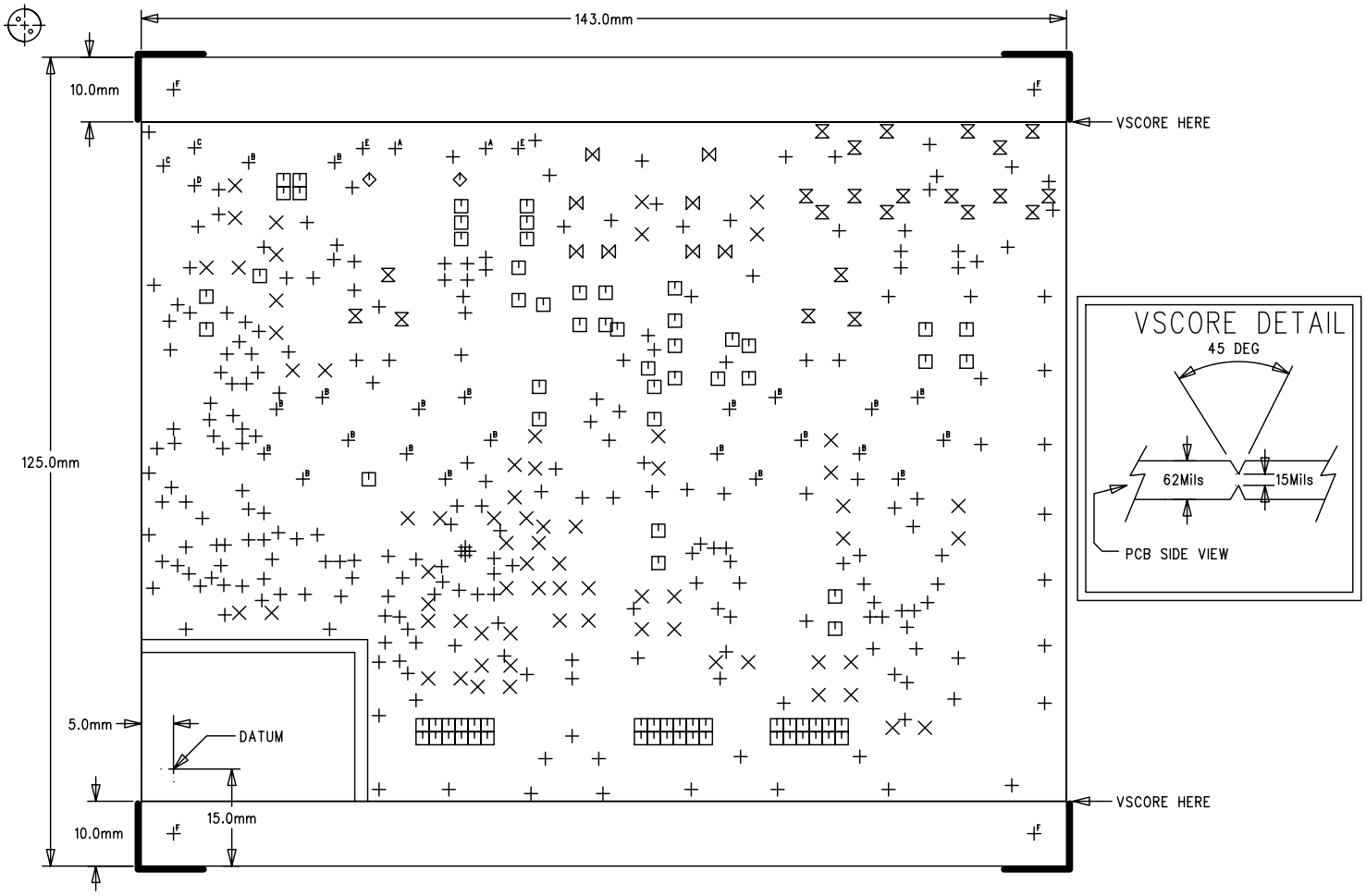


ALESIS 9-40-0350-C "TOPTRACE"



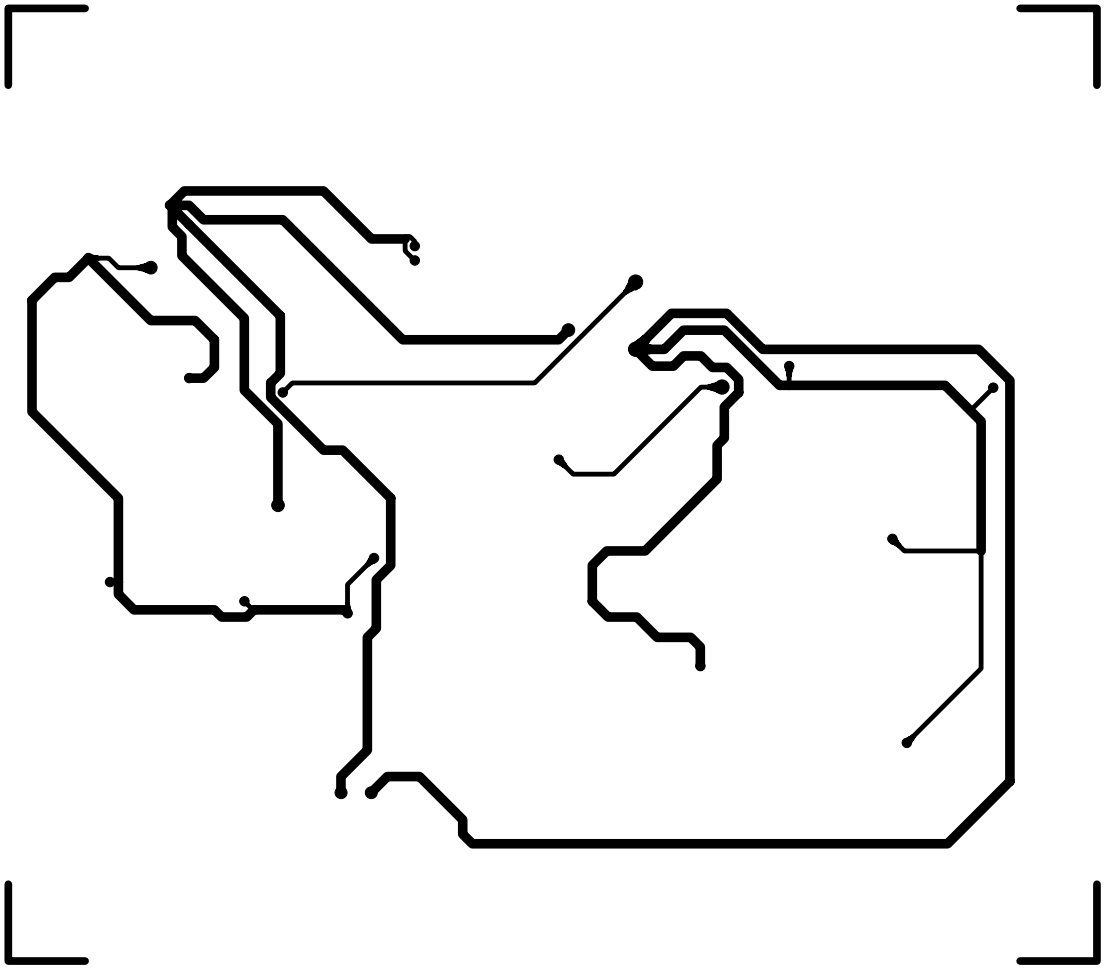
ALESIS 9-40-0350-C "GNDPLANE LAYER 2"

ALESIS 9-40-0350-C "DRILLDWG"

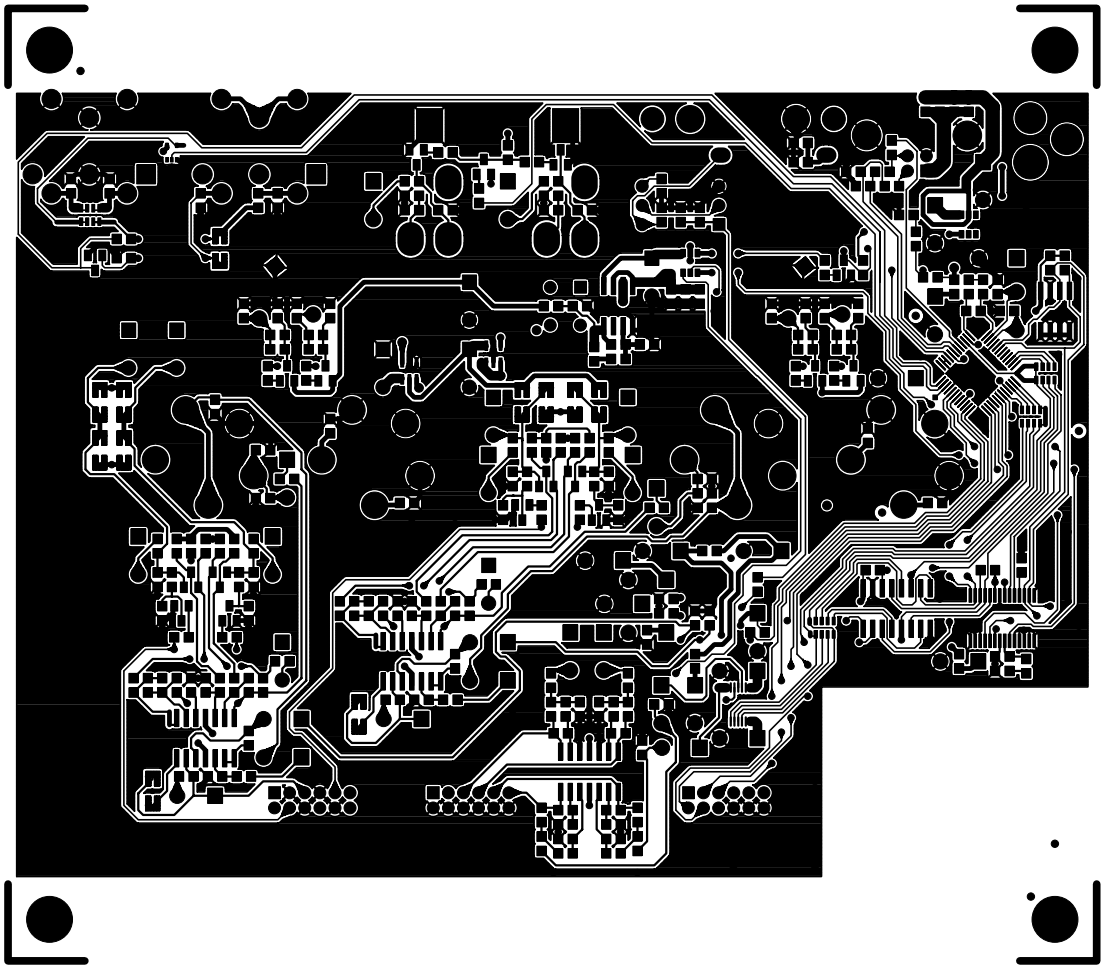


SIZE	QTY	SYM	PLATED	TOL
20	241	+	YES	+/-3
25	68	X	YES	+/-3
37	79	□	YES	+/-3
47.2	2	◇	YES	+/-3
51.2	22	⧖	YES	+/-3
82.7	8	⋈	YES	+/-3
86.6	2	+A	YES	+/-3
90.6	22	+B	YES	+/-3
100.4	2	+C	YES	+/-3
125	1	+D	YES	+/-3
126	2	+E	NO	+/-3
157.5	4	+F	YES	+/-3

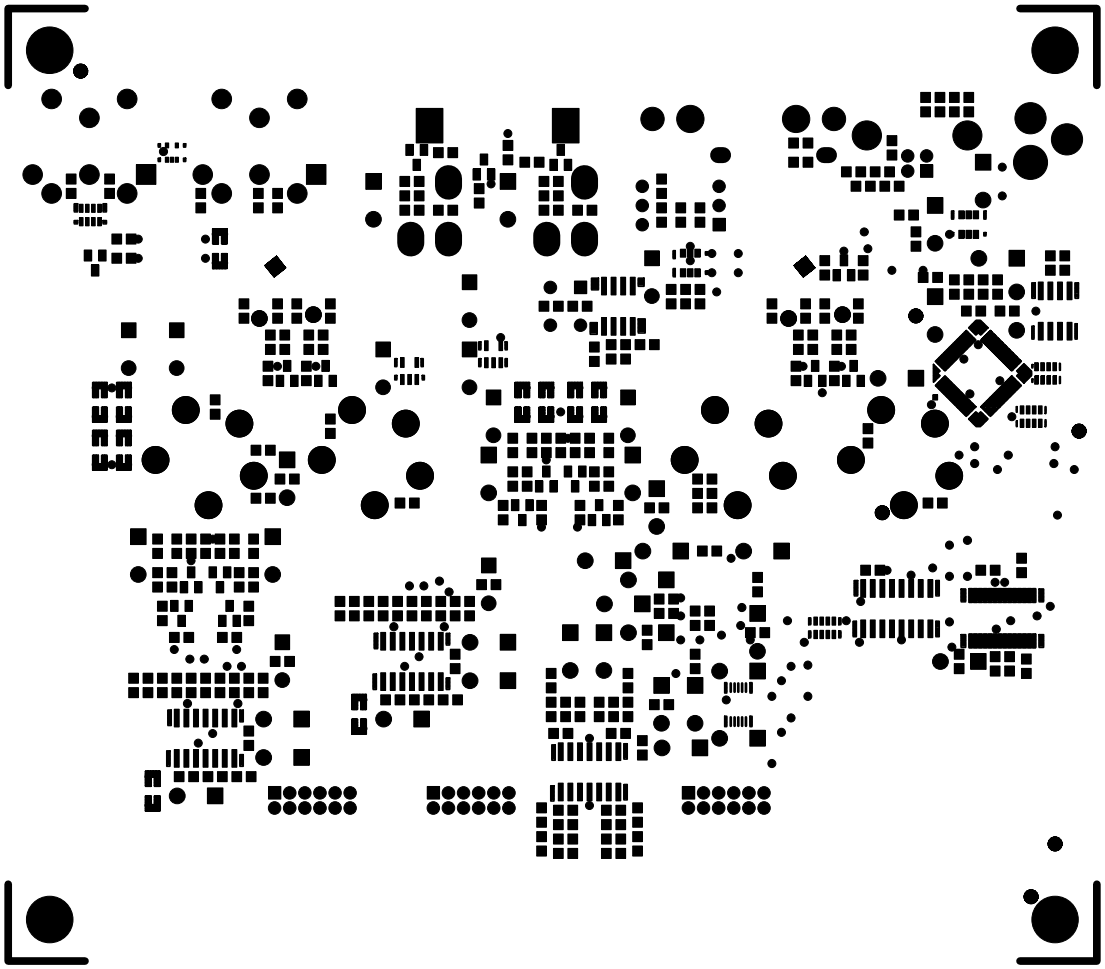
1. Design rules used: 0.008" lines. 0.008" space
2. 4-layer design.
3. Surface-mount parts on top and bottom sides.
4. Material: 0.062" (+/- 0.007") thick glass epoxy FR-4 (green) 1 oz. copper all layers, finished.
5. Finish: SMOBC, Hot Air Level
6. Hole sizes are finished diameter after plating with 0.0010" minimum plating all surfaces. (Except 20 mil via whose finished size is unimportant.) Drilled holes are +/- 0.003" tolerance.
7. Layer-to-layer registration to be +/-0.005"
8. Soldermask all exposed copper, LPI, GREEN color.
9. Silkscreen using epoxy-based ink (white).
10. Surface to be flat within 0.010" in/in of diagonal measurement.
11. Vendor shall etch, silkscreen or stamp I.D. logo and date code, type designation and UL flame rating on top side of PCB. NO COPPER MAY BE DELETED
12. Soldercoat both sides to standard J-STD-003.
13. Finished pcb shall have 0.0035" min dielectric material between consecutive conductor layers when cured.
14. Mechanical dims are +/- 0.005" tolerance.
15. Workmanship and acceptance criteria shall be in accordance with IPC-A-600, Class 1.



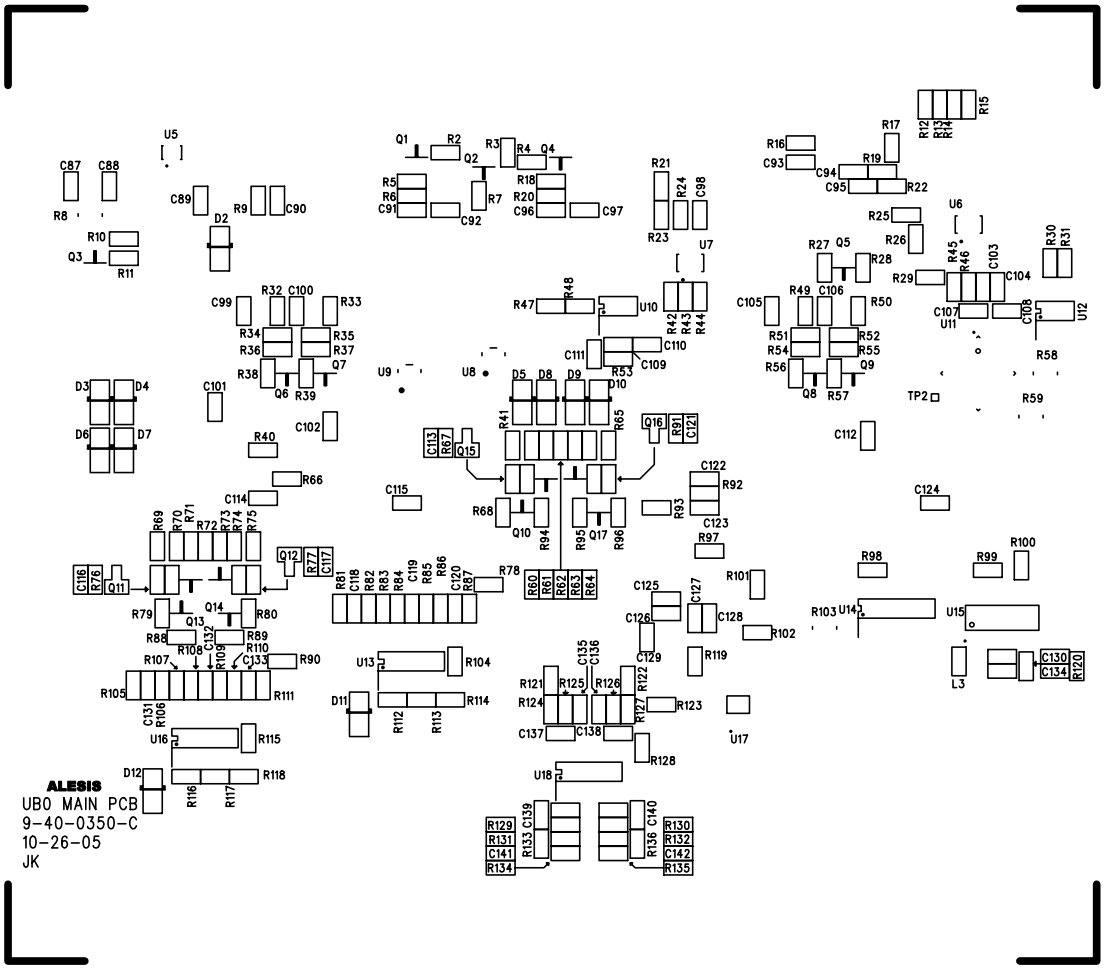
ALESIS 9-40-0350-C "PWRPLANE LAYER 3"



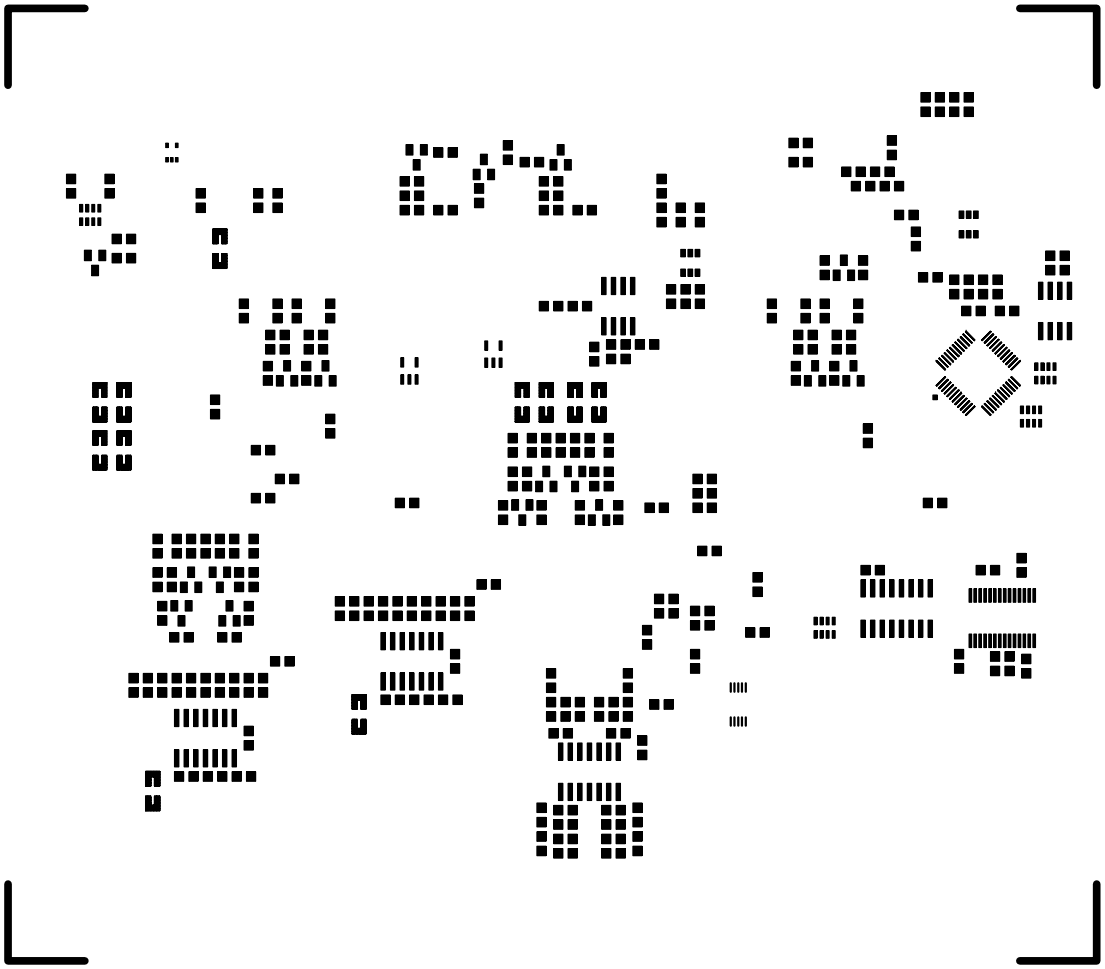
ALESIS 9-40-0350-C "BOTTRACE"



ALESIS 9-40-0350-C "BOTSMK"

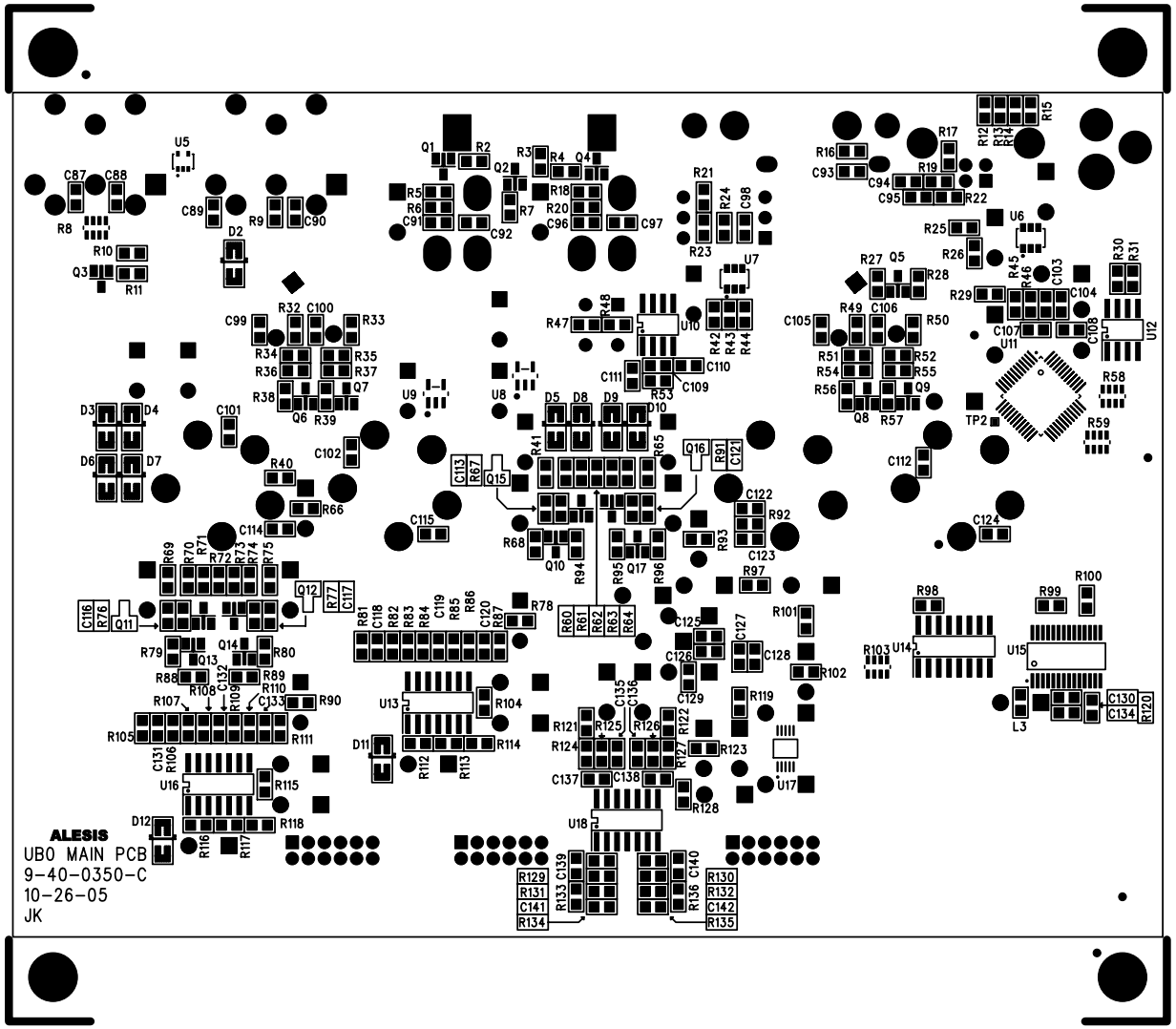


ALESIS 9-40-0350-C "BOTSILK"



ALESIS 9-40-0350-C "BOTPASTE"

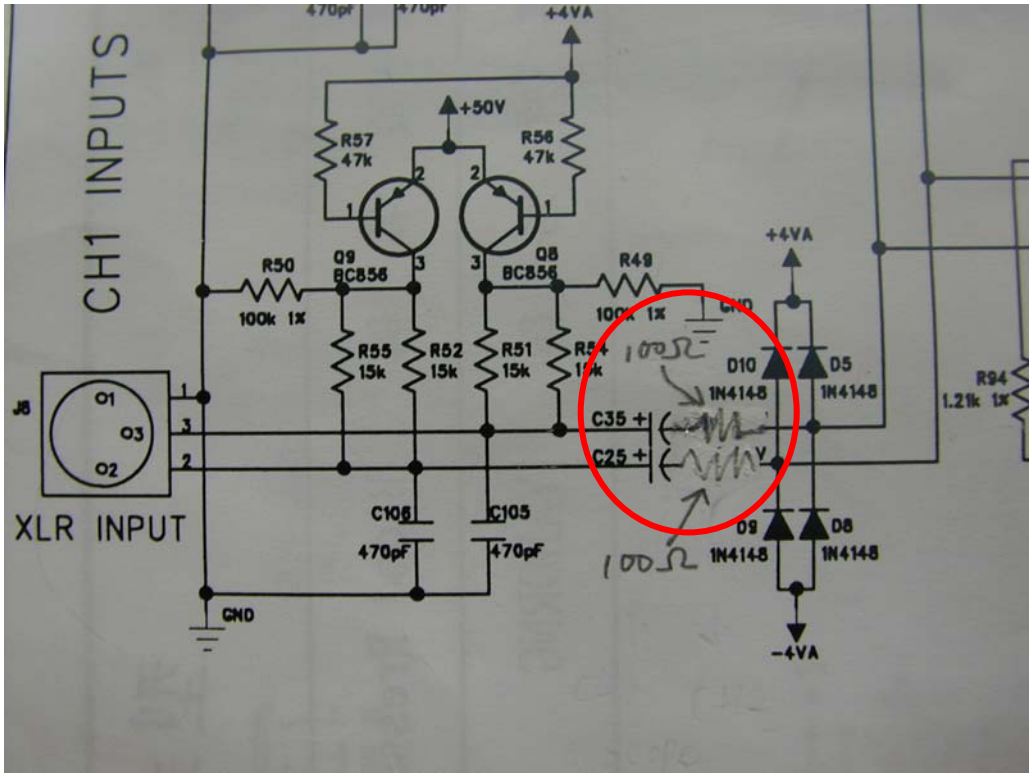
ALESIS 9-79-0350-C "BOTTOM ASSEMBLY DRAWING"



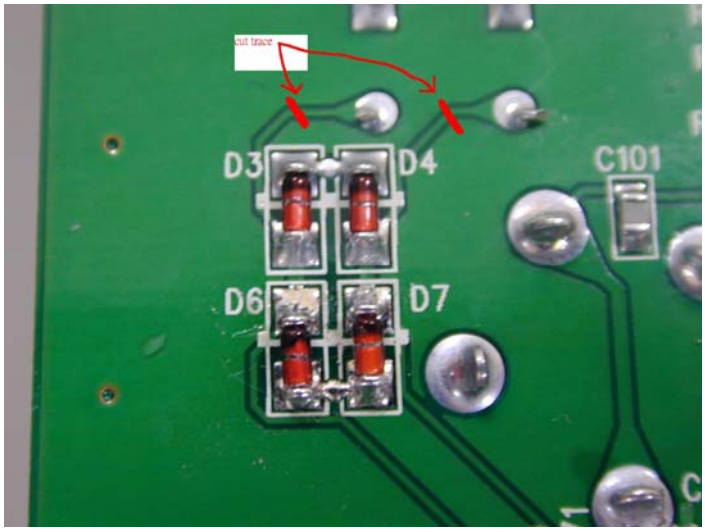
	UB0MNC - Main PCB Rev C						**Last Revised:**	
	RevChange Document						**10/26/2005**	
SCH	**PCB**	**CAM**	**Suggested by:**	**DATE**	**Performed by:**	**DATE**	**Description of change:**	**Reason for change:**
							TOP LEVEL CHANGES	
x	x		SOP	10/12/2005	JK	10/26/2005	Change all text from Rev B to C	SOP
x	x		SOP	10/12/2005	JK	10/26/2005	update all Part Types	SOP
			SOP	10/12/2005			Review/Integrate all outstanding ECNs	SOP
							Note: ***A new solderpaste stencil IS required***	A component was removed.
x	x		YHT	10/12/2005	JK	10/26/2005	Ground the USB shield directly to GND instead of through ferrite bead. Remove ferrite bead L2.	EMC compliance.
							SCHEMATIC CHANGES	
							PCB CHANGES	

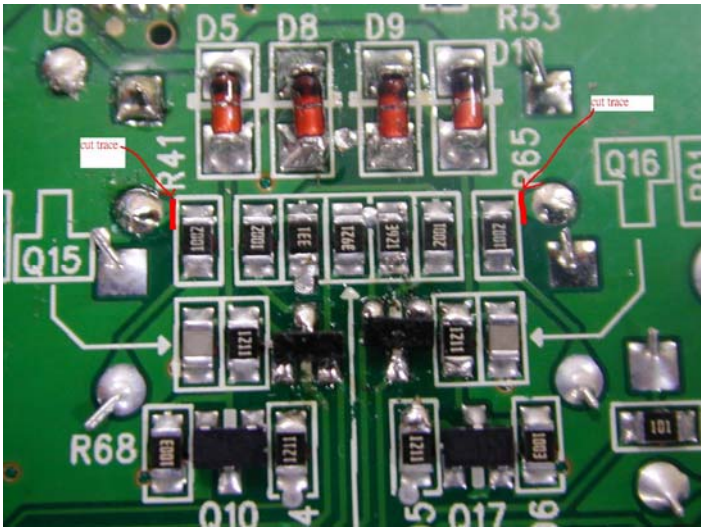
UB0 Main PCB Rev.C Modifications

Insert 100ohm resistor in series with each of the DC blocking caps for the CH1 and CH2 input (C25, C30, C31, and C35).

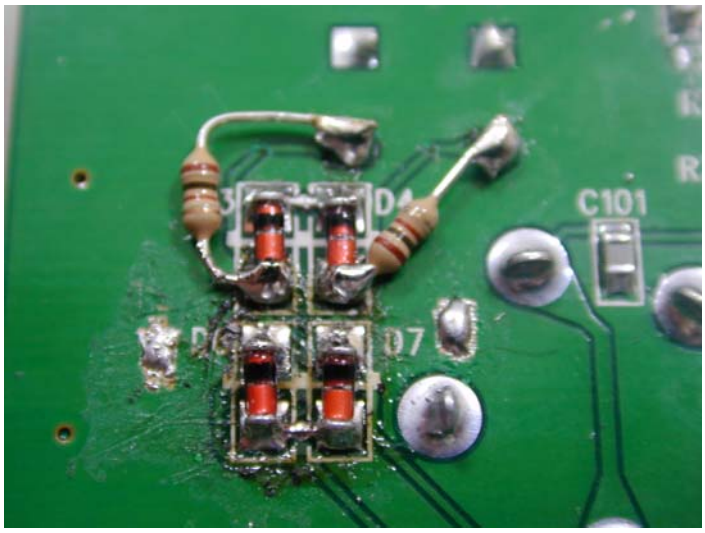


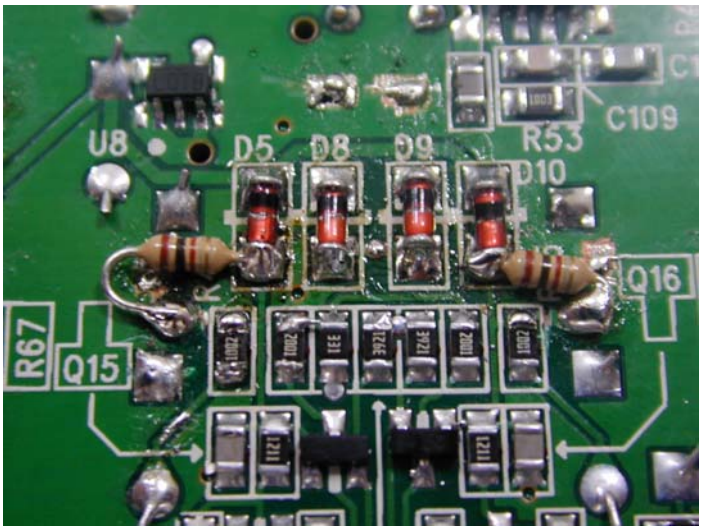
Cut PCB traces (4 places) as indicated below:





Solder a 100ohm resistor onto PCB to bridge the cut (4 places):



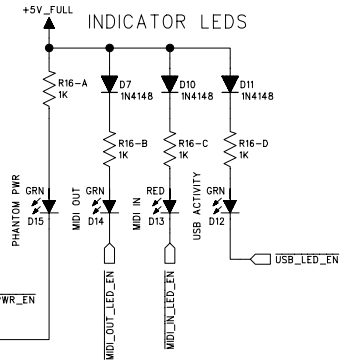


FRONT PANEL PCB

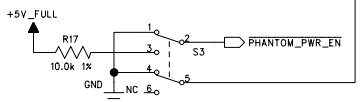
REV C

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

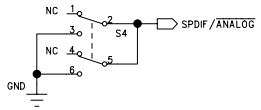
INDICATOR LEDS

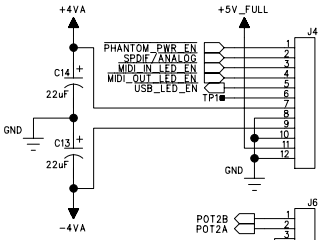


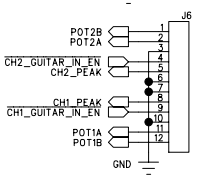
PHANTOM POWER ENABLE

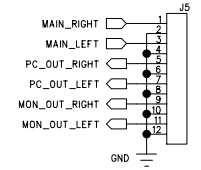


INPUT SELECT SWITCH



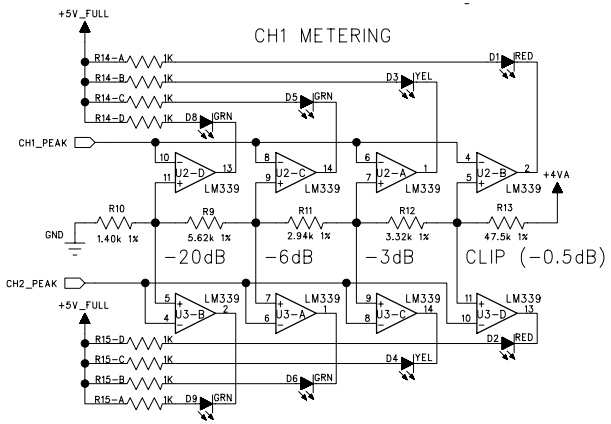




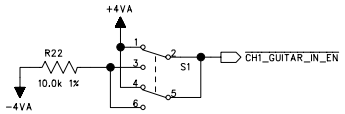


TO MAIN PCB

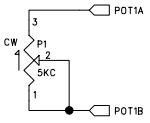
CH1 METERING



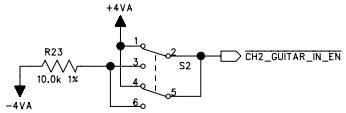
CH1 GUITAR INPUT ENABLE



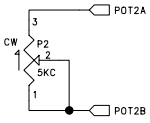
CH1 GAIN



CH2 GUITAR INPUT ENABLE



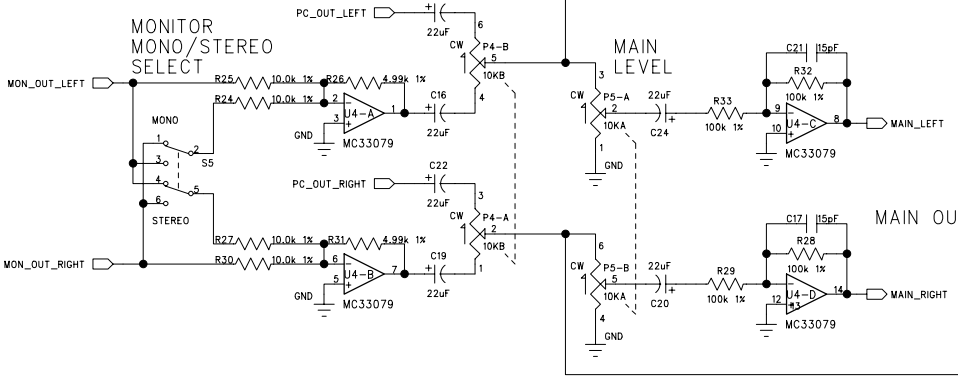
CH2 GAIN



CH2 METERING

DIRECT/USB BALANCE

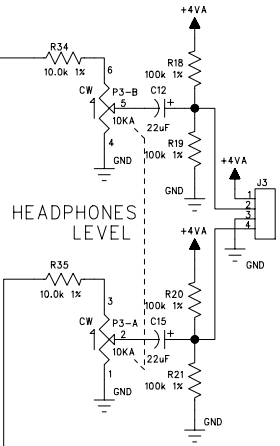
MONITOR MONO/STEREO SELECT

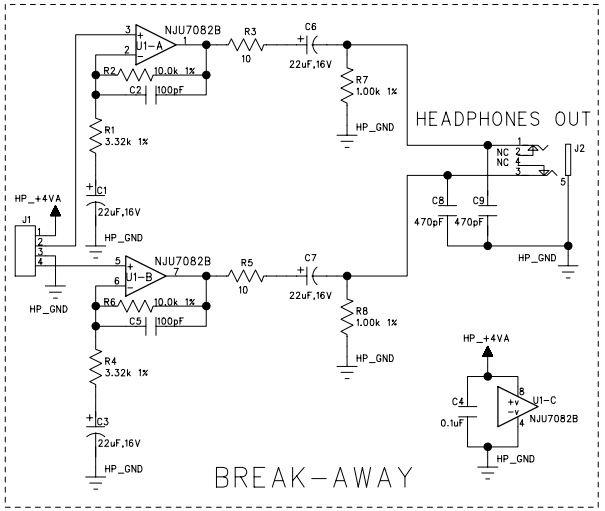


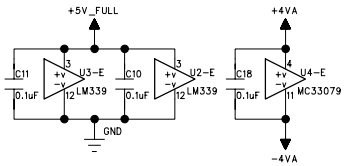
MAIN LEVEL

MAIN OUTS

HEADPHONES LEVEL

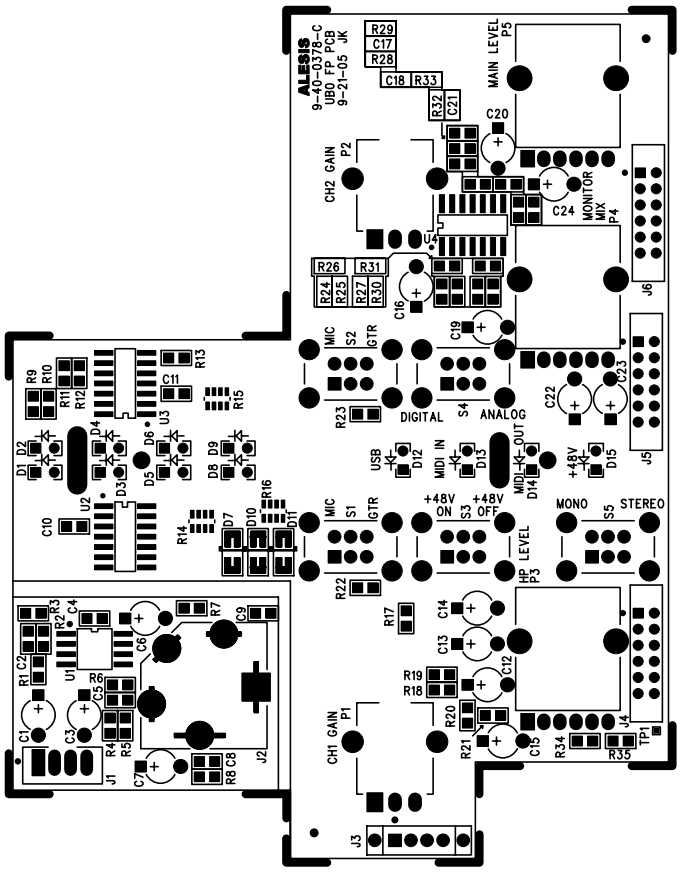


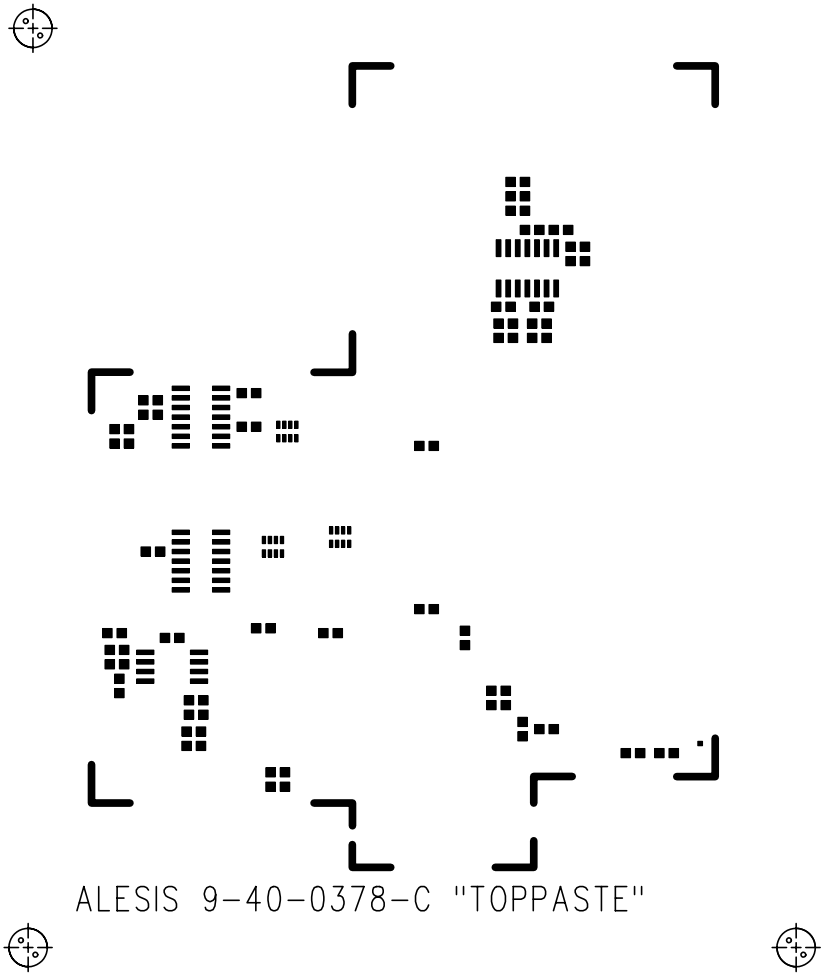




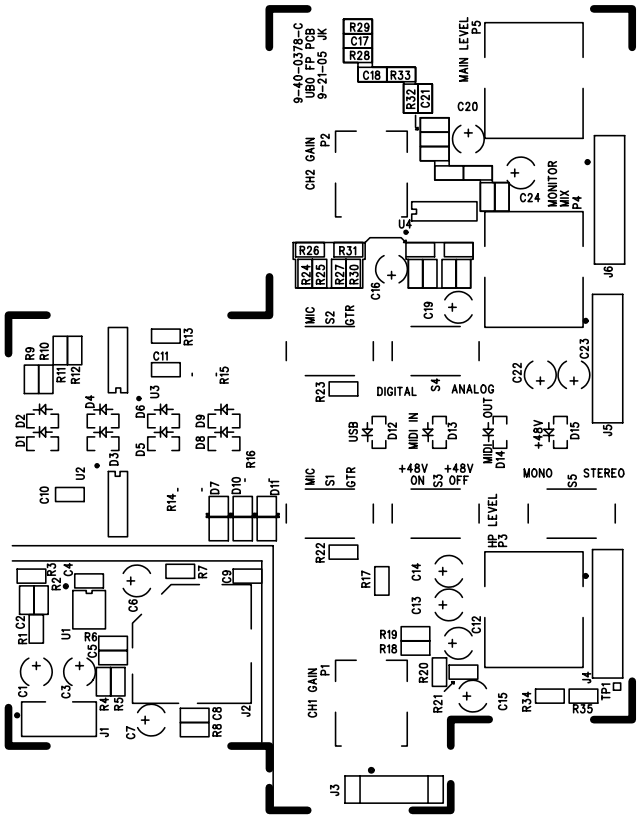
COMPANY:	ALESIS		
TITLE:	UBO FRONT PANEL PCB		
PART NUMBER:	9-40-0378-C	REV: B	
ASSY NUMBER:	9-79-0378		
FILENAME:	UB0FPB01C.SCH	SIZE: C	
SCALE:		SHEET: 1 OF 1	
DRAWN: P MARESH/JKHO/AWS	DATED: 11/2005		
RELEASED:	DATED:		

ALESIS 9-79-0378-C "TOP ASSEMBLY DRAWING"

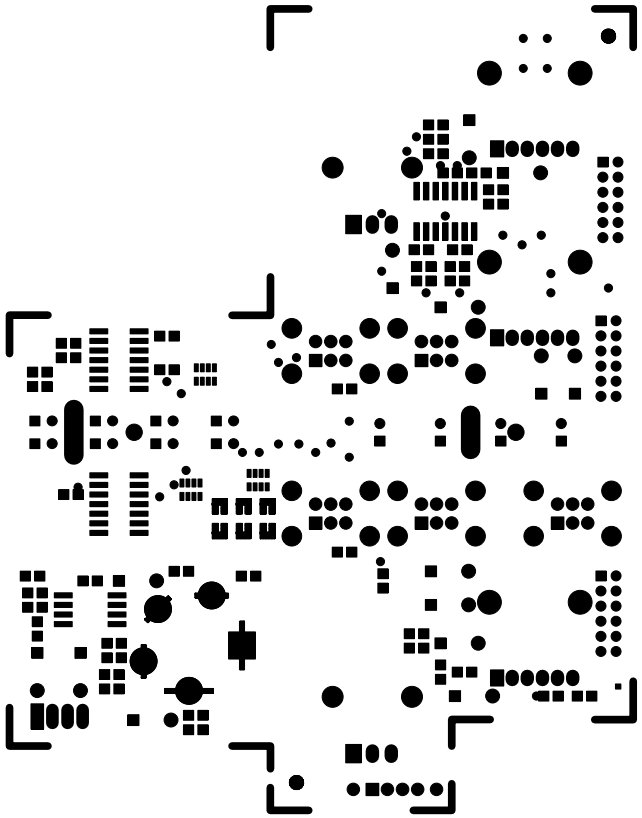




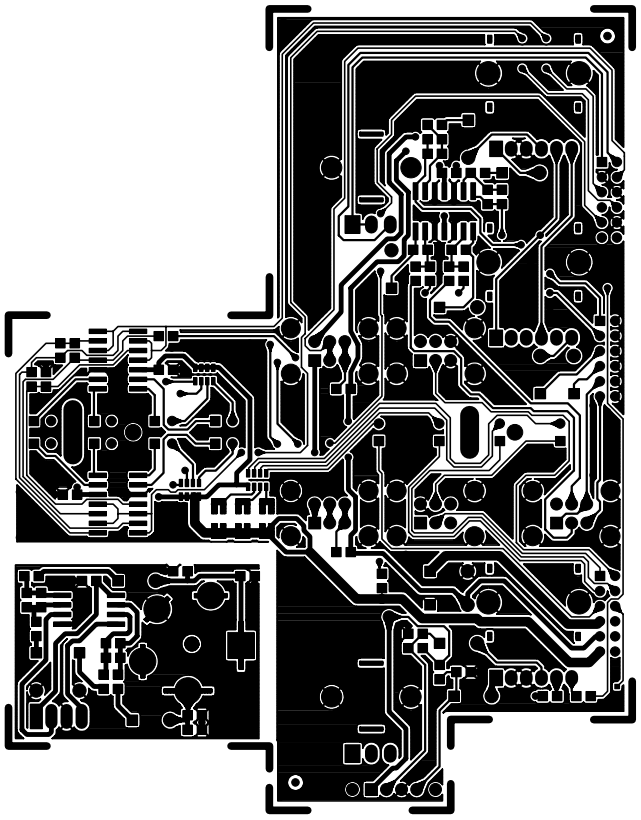
ALESIS 9-40-0378-C "TOPPASTE"



ALESIS 9-40-0378-C "TOPSILK"

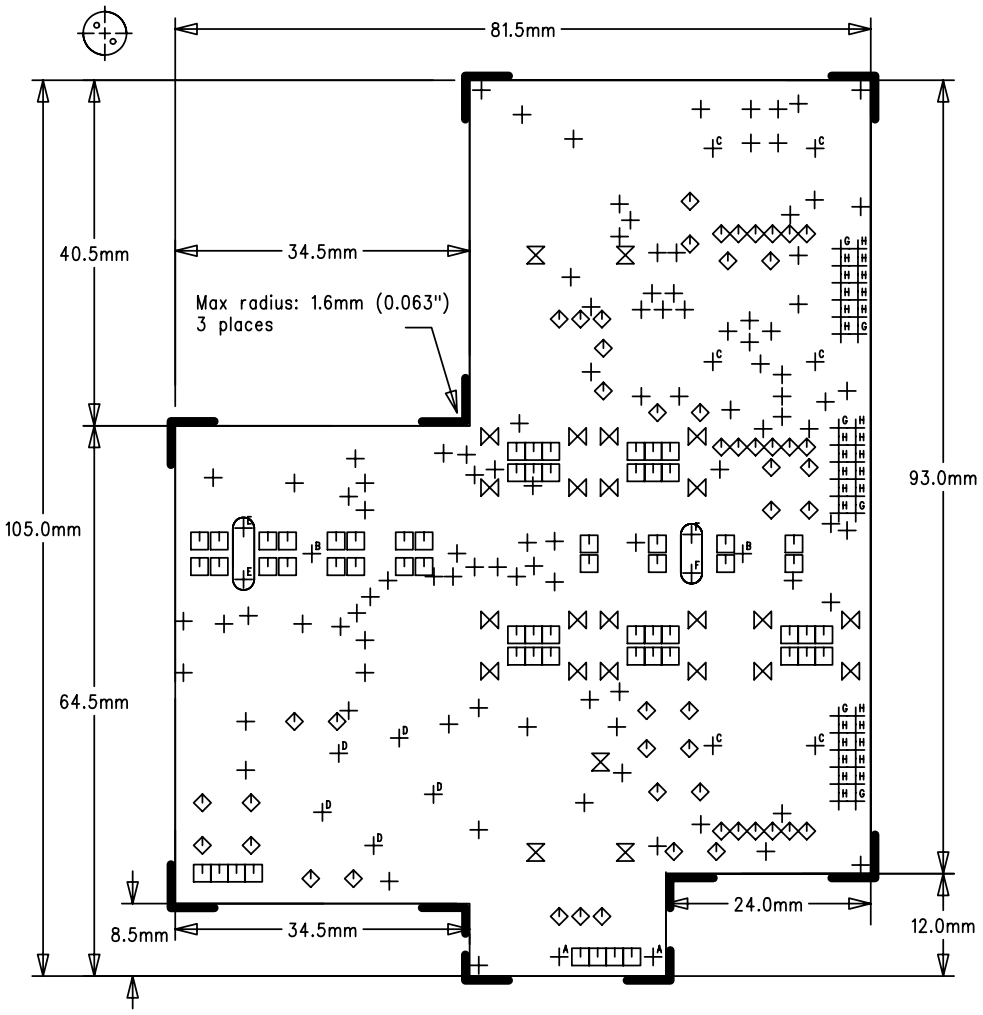


ALESIS 9-40-0378-C "TOPSMK"



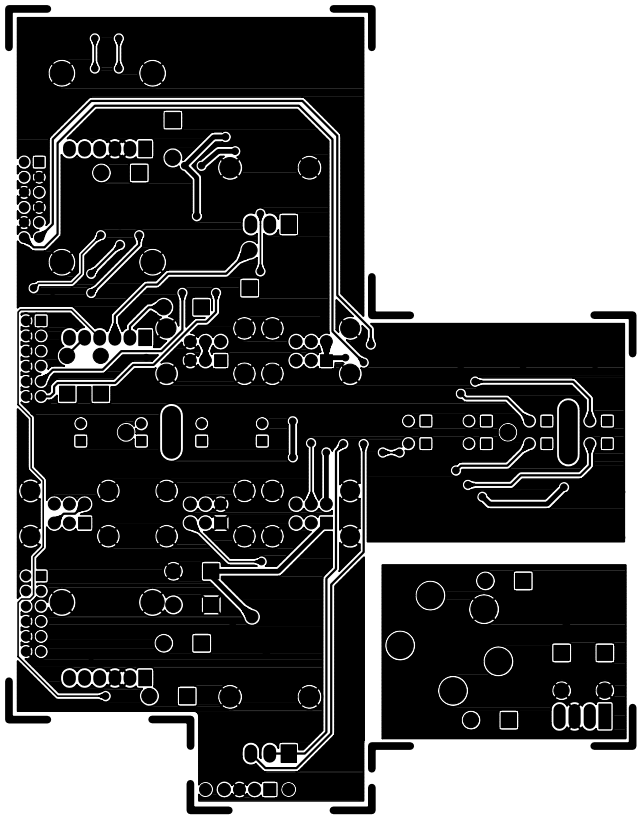
ALESIS 9-40-0378-C "TOPTRACE"

ALESIS 9-40-0378-C "DRILLDWG"

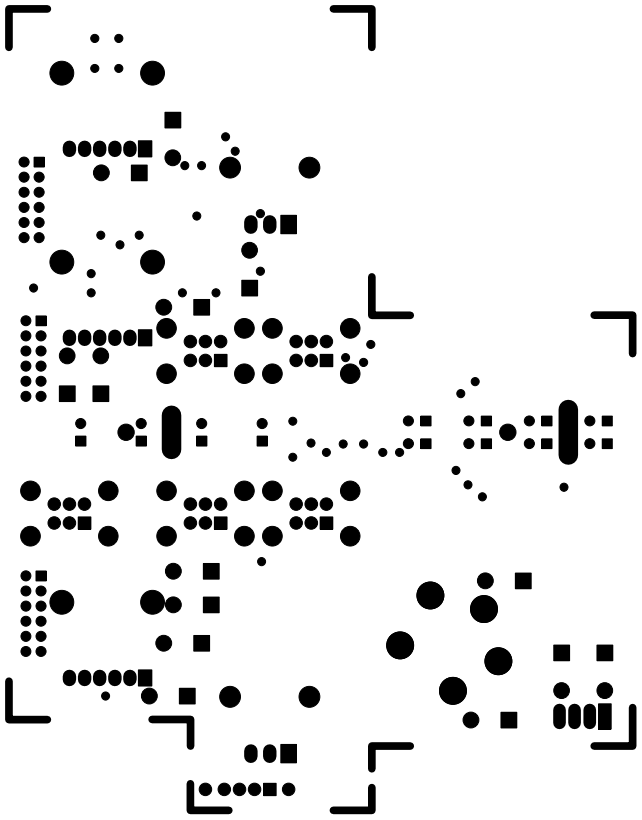


SIZE	QTY	SYM	PLATED	TOL
20	101	+	YES	+/-3.0
31.5	62	□	YES	+/-3.0
39.4	52	◇	YES	+/-3.0
47.2	5	⧖	YES	+/-3.0
63	20	⋈	YES	+/-3.0
63	2	+A	NO	+/-3.0
82.7	2	+B	NO	+/-3.0
82.7	6	+C	YES	+/-3.0
90.6	5	+D	YES	+/-3.0
98.4 x 335	1	+E	NO	+/-3.0
98.4 x 276	1	+F	NO	+/-3.0
21.6	6	+G	YES	+/-0.0
23.6	30	+H	YES	+/-0.0

1. Design rules used: 0.008" lines. 0.008" space
2. Two-layer design.
3. Surface-mount parts on top side only.
4. Material: 0.062" (+/- 0.007") thick glass epoxy FR-4 (green) 1 oz. copper all layers, finished.
5. Finish: SMOBC, Hot Air Level
6. Hole sizes are finished diameter after plating with 0.0010" minimum plating all surfaces. (Except 20-mil via whose finished size is unimportant.) Drilled holes are +/- 0.003" tolerance.
7. Layer-to-layer registration to be +/-0.005"
8. Soldermask all exposed copper, LPI, GREEN color.
9. Silkscreen using epoxy-based ink (white).
10. Surface to be flat within 0.010" in/in of diagonal measurement.
11. Vendor shall etch, silkscreen or stamp I.D. logo and date code, type designation and UL flame rating on top side of PCB. NO COPPER MAY BE DELETED
12. Soldercoat both sides to standard J-STD-003.
13. Finished pcb shall have 0.0035" min dielectric material between consecutive conductor layers when cured.
14. Mechanical dims are +/- 0.005" tolerance.
15. Workmanship and acceptance criteria shall be in accordance with IPC-A-600, Class 1.



ALESIS 9-40-0378-C "BOTTRACE"



ALESIS 9-40-0378-C "BOTSMK"

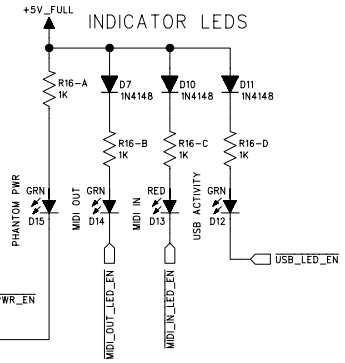
	UB0FPA - Front Panel PCB Rev C						**Last Revised:**	
	RevChange Document						**11/28/2005**	
SCH	**PCB**	**CAM**	**Suggested by:**	**DATE**	**Performed by:**	**DATE**	**Description of change:**	**Reason for change:**
							TOP LEVEL CHANGES	
			SOP	9/21/2005			Change revision to Rev C	SOP
			SOP	9/21/2005			Update all Part Types	SOP
			SOP	9/21/2005			Review/Integrate all outstanding ECNs	SOP
	x		AWS	11/20/2005	AWS	11/28/2005	Resize drill hole in ribbon cables' footprints	Yahourng Request
	x		AWS	11/28/2005	AWS	11/28/2005	Modify footprint of 1-08-0222 for 1mm hole size	Yahourng request
x	x		MBL	9/26/2005	AWS	11/20/2005	Change headphone volume control from post-Main volume to pre, so that the Main and Headphone volumes are independent.	Multiple user requests.
							Note: ***A new solderpaste stencil IS/IS NOT required***	
							SCHEMATIC CHANGES	
							PCB CHANGES	

FRONT PANEL PCB

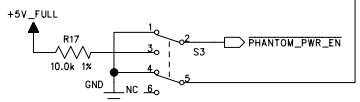
REV B

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

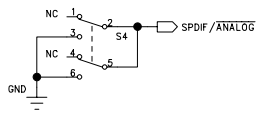
INDICATOR LEDS

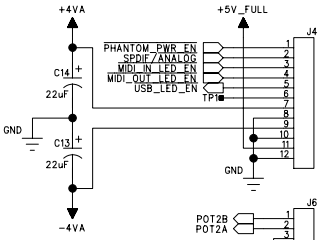


PHANTOM POWER ENABLE



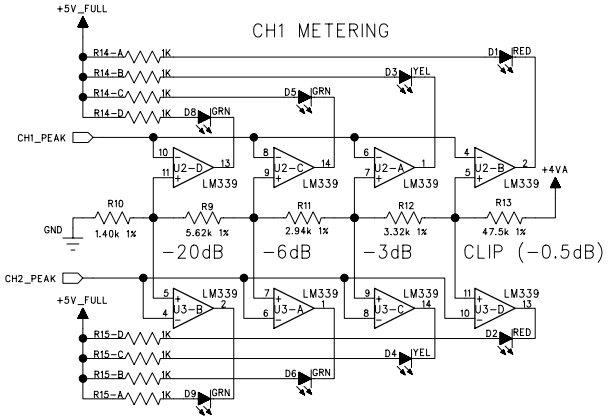
INPUT SELECT SWITCH



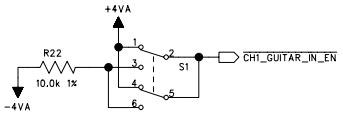


TO MAIN PCB

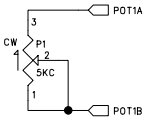
CH1 METERING



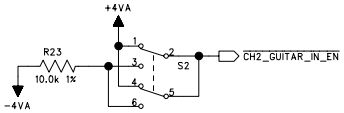
CH1 GUITAR INPUT ENABLE



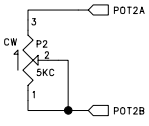
CH1 GAIN



CH2 GUITAR INPUT ENABLE



CH2 GAIN



CH2 METERING

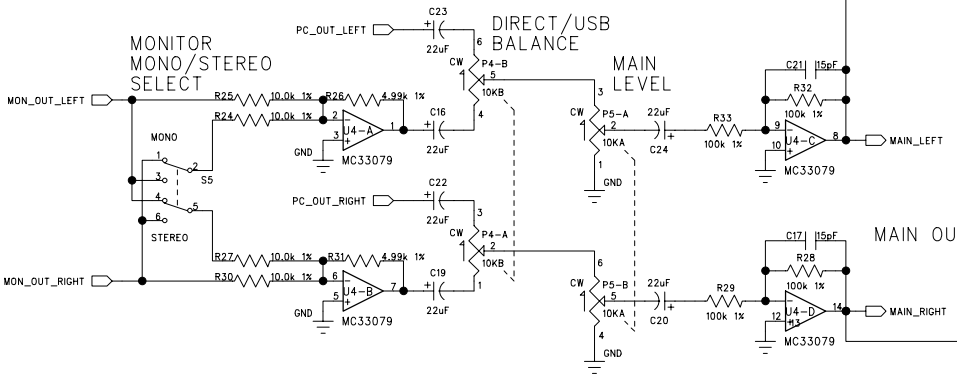
MONITOR MONO/STEREO SELECT

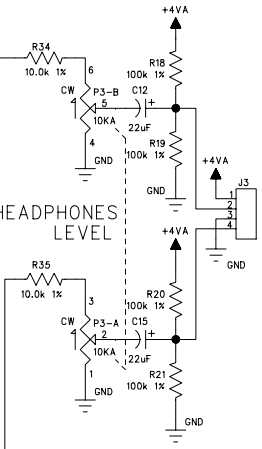
DIRECT/USB BALANCE

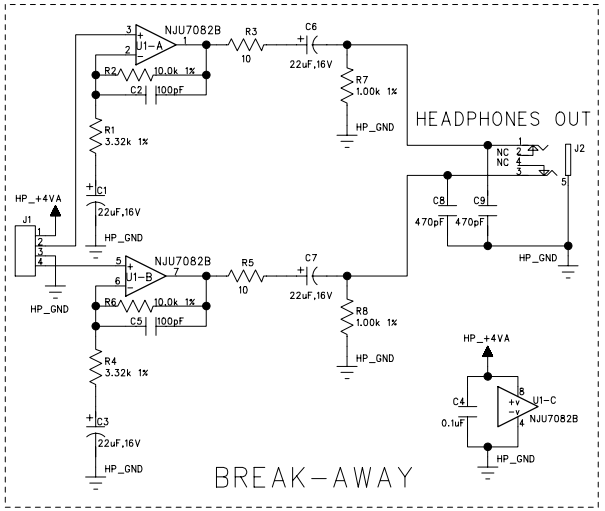
MAIN LEVEL

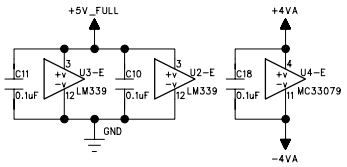
HEADPHONES LEVEL

MAIN OUTS



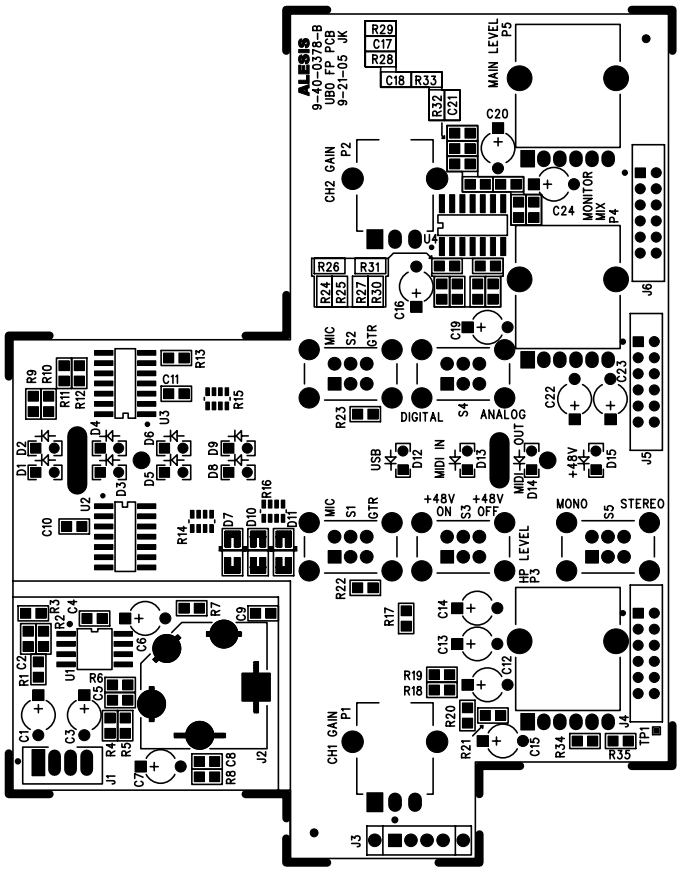


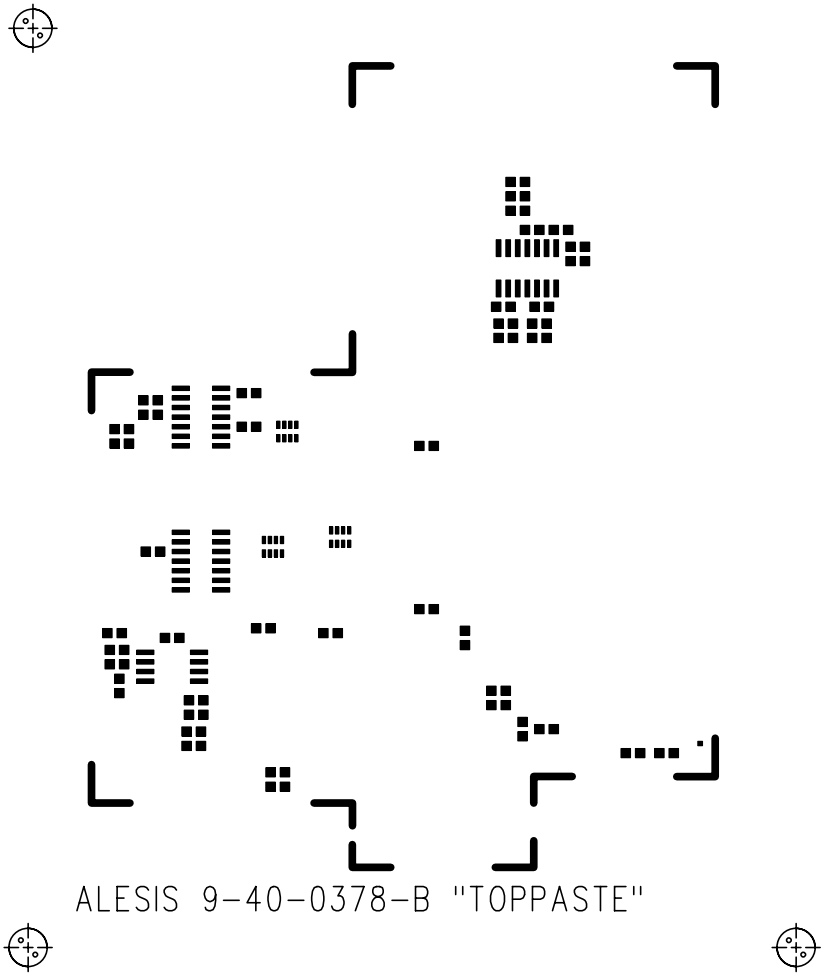




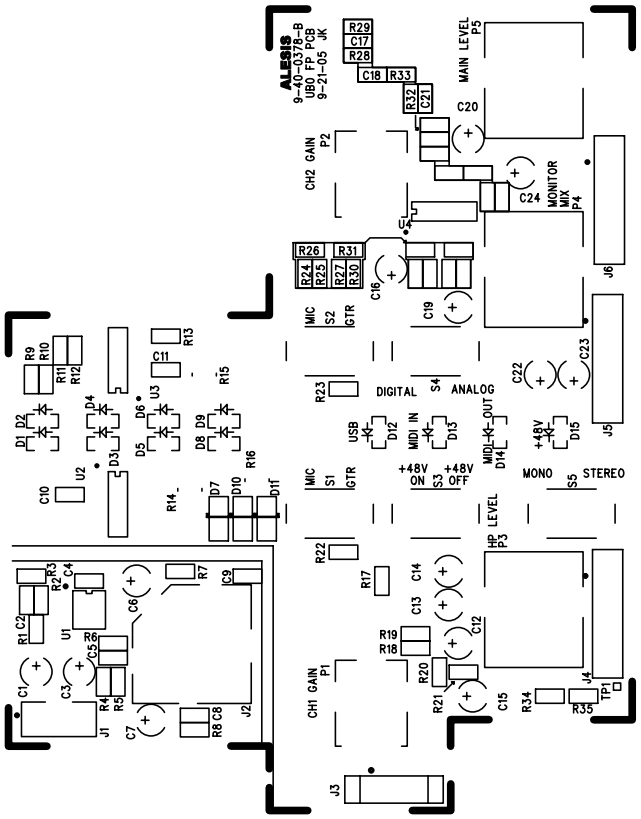
COMPANY:	ALESIS		
TITLE:	UBO FRONT PANEL PCB		
PART NUMBER:	9-40-0378-B	REV: B	
ASSY NUMBER:	9-79-0378		
FILENAME:	UB0FPB01A.SCH	SIZE: C	
SCALE:		SHEET: 1 OF 1	
DRAWN: P MARESH/JKHO	DATED: 9/2005		
RELEASED:	DATED:		

ALESIS 9-79-0378-B "TOP ASSEMBLY DRAWING"

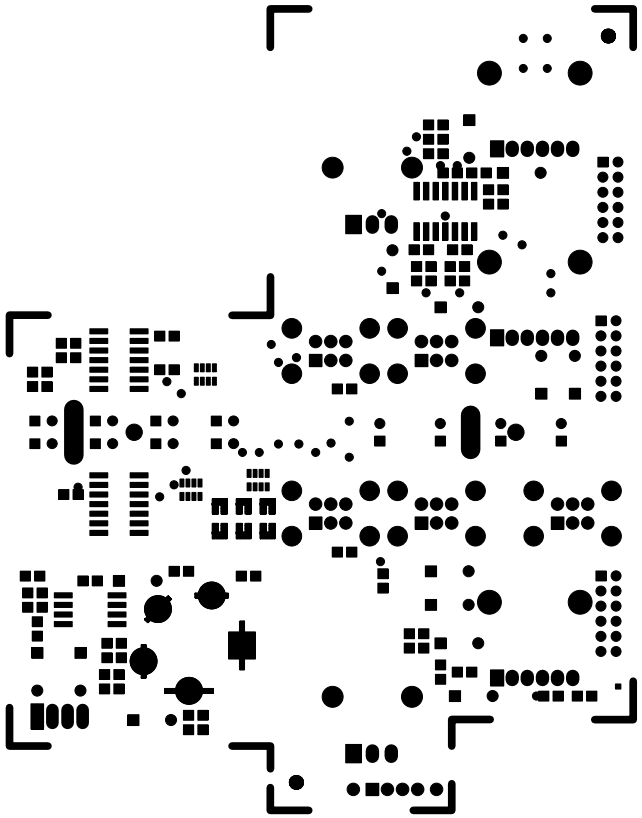




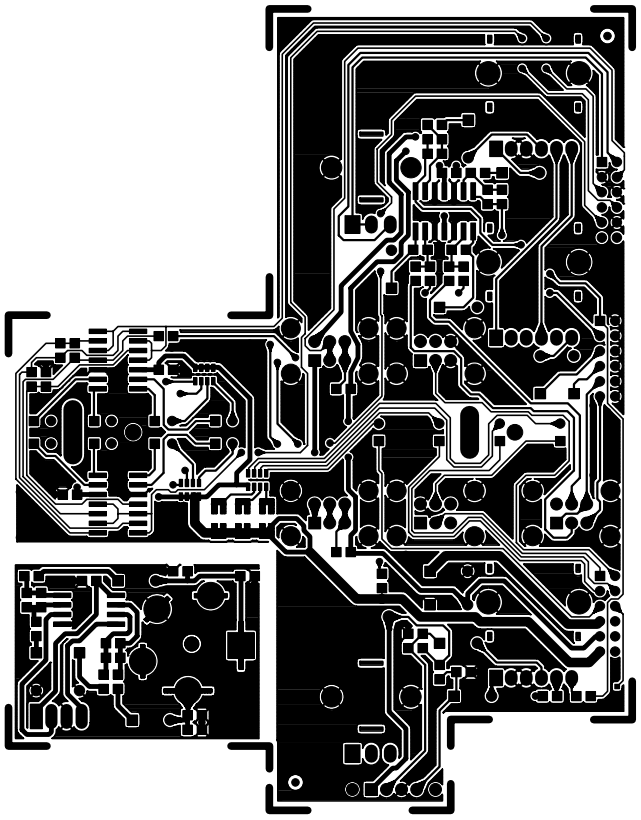
ALESIS 9-40-0378-B "TOPPASTE"



ALESIS 9-40-0378-B "TOPSILK"

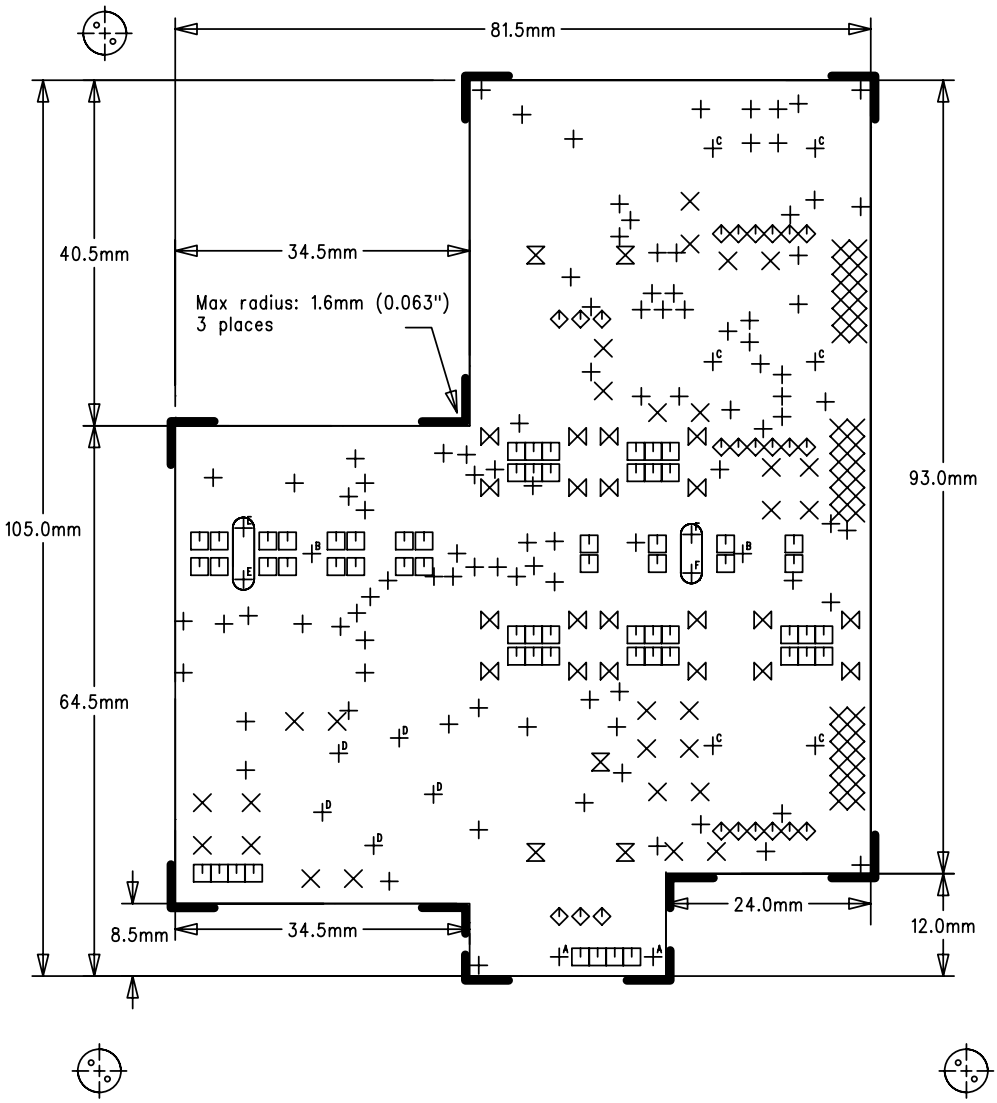


ALESIS 9-40-0378-B "TOPSMK"



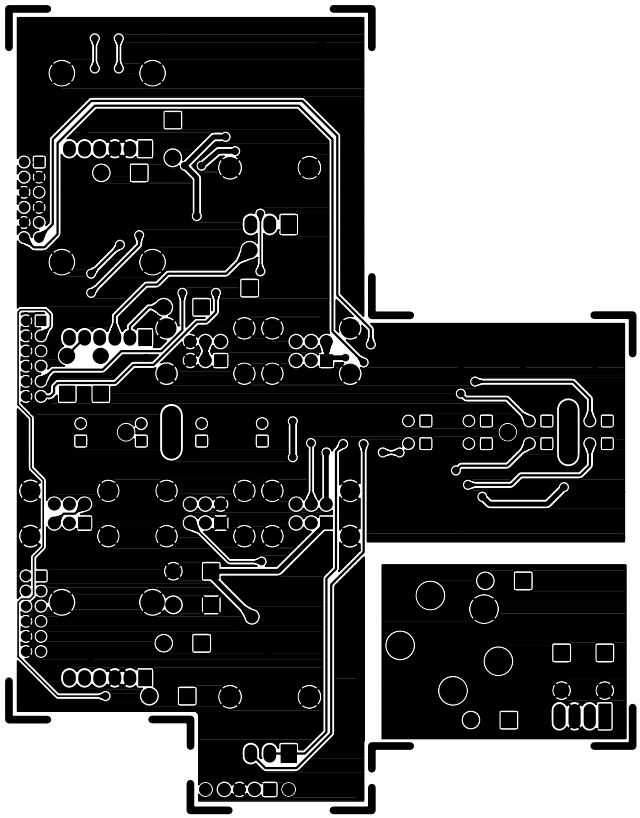
ALESIS 9-40-0378-B "TOPTRACE"

ALESIS 9-40-0378-B "DRILLDWG"

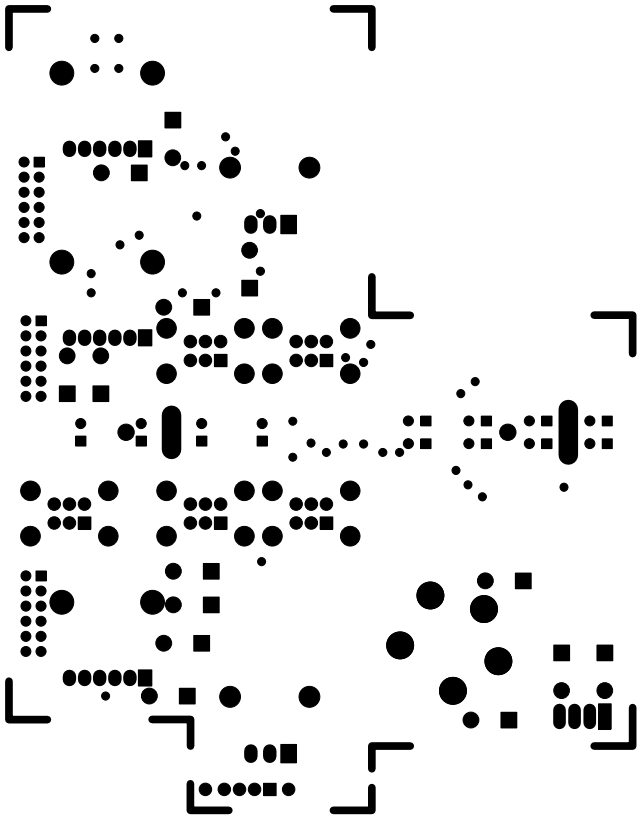


SIZE	QTY	SYM	PLATED	TOL
20	98	+	YES	+/-3.0
25	64	X	YES	+/-3.0
31.5	62	□	YES	+/-3.0
39.4	24	◇	YES	+/-3.0
47.2	5	⧖	YES	+/-3.0
63	20	⋈	YES	+/-3.0
63	2	+A	NO	+/-3.0
82.7	2	+B	NO	+/-3.0
82.7	6	+C	YES	+/-3.0
90.6	5	+D	YES	+/-3.0
98.4 x 335	1	+E	NO	+/-3.0
98.4 x 276	1	+F	NO	+/-3.0

1. Design rules used: 0.008" lines. 0.008" space
2. Two-layer design.
3. Surface-mount parts on top side only.
4. Material: 0.062" (+/- 0.007") thick glass epoxy FR-4 (green) 1 oz. copper all layers, finished.
5. Finish: SMOBC, Hot Air Level
6. Hole sizes are finished diameter after plating with 0.0010" minimum plating all surfaces. (Except 20-mil via whose finished size is unimportant.) Drilled holes are +/- 0.003" tolerance.
7. Layer-to-layer registration to be +/-0.005"
8. Soldermask all exposed copper, LPI, GREEN color.
9. Silkscreen using epoxy-based ink (white).
10. Surface to be flat within 0.010" in/in of diagonal measurement.
11. Vendor shall etch, silkscreen or stamp I.D. logo and date code, type designation and UL flame rating on top side of PCB. NO COPPER MAY BE DELETED
12. Soldercoat both sides to standard J-STD-003.
13. Finished pcb shall have 0.0035" min dielectric material between consecutive conductor layers when cured.
14. Mechanical dims are +/- 0.005" tolerance.
15. Workmanship and acceptance criteria shall be in accordance with IPC-A-600, Class 1.



ALESIS 9-40-0378-B "BOTTRACE"



ALESIS 9-40-0378-B "BOTSMK"

	UB0FPB - Front Panel PCB Rev B						**Last Revised:**	
	RevChange Document						**9/21/2005**	
SCH	**PCB**	**CAM**	**Suggested by:**	**DATE**	**Performed by:**	**DATE**	**Description of change:**	**Reason for change:**
							TOP LEVEL CHANGES	
			SOP	9/20/2005	JK	9/21/2005	Change revision to Rev B	SOP
			SOP	9/20/2005			Update all Part Types	SOP
			SOP	9/20/2005			Review/Integrate all outstanding ECNs	SOP
							Note: ***A new solderpaste stencil IS NOT required***	No components are changed.
							SCHEMATIC CHANGES	
							PCB CHANGES	
			JK	9/20/2005	JK	9/21/2005	Increase hole size for LEDs.	Current hole size is just a little tight, which would make manufacturing more difficult.

ALESIS
IO|2 (UB0)

ECN
HISTORY

ALESIS

ENGINEERING CHANGE NOTICE

DOCUMENT CONTROL RELEASE 3/17/06 APPROVAL ALESIS J.K.

ECN #: LG07604 **PRODUCT(S):** UB0

DATE: 3/17/06 **ASSEMBLY(S):** 9-79-0350-F0

CHANGE TO BE MADE

WAS

9-40-0350-E PCB MAIN UB0 – REV E

IS

9-40-0350-F PCB MAIN UB0 – REV F

REASON FOR CHANGE:

The leads of certain thru-hole components were shorting to adjacent pads after going through wave-soldering. The offending components were moved farther apart prevent the shorts from occurring.

SPECIAL INSTRUCTIONS:

Number of pages attached: 0

MATERIAL DISPOSITION: Mark "X" on all that apply...

	USE AS IS	APPLY CHANGE(S)	SCRAP
ON ORDER		x	
WIP	x		
STOCK	x		
RETURNS	x		

PROJECT ENGINEER: _____

MANF. ENGINEER: / DIRECTOR'S INITS. _____

BOM UPDATED: ___/___/___

UPDATED BY: _____

WORK ORDER UPDATED: ___/___/___

COORDINATOR: _____

ALESIS

ENGINEERING CHANGE NOTICE

DOCUMENT CONTROL RELEASE 3/15/06 APPROVAL J.K.

ECN #: LG07401 **PRODUCT(S):** UB0

DATE: 3/15/06 **ASSEMBLY(S):** 9-79-0350-E0

CHANGE TO BE MADE

WAS

9-40-0350-D PCB MAIN UB0 – REV D

IS

9-40-0350-E PCB MAIN UB0 – REV E

REASON FOR CHANGE:

The current rev D PCB does not implement the input protection circuitry properly. Rev E fixes this problem.

SPECIAL INSTRUCTIONS:

Number of pages attached: 0

MATERIAL DISPOSITION: Mark "X" on all that apply...

	USE AS IS	APPLY CHANGE(S)	SCRAP
ON ORDER		x	
WIP	x		
STOCK	x		
RETURNS	x		

PROJECT ENGINEER:

MANF. ENGINEER: / DIRECTOR'S INITS.

BOM UPDATED: ___/___/___

UPDATED BY:

WORK ORDER UPDATED: ___/___/___

COORDINATOR:

ALESIS
IO|2 (UB0)

BOM

UB0 BOM

September 22, 2005

Note: Vendor is free to add/change/delete hardware (screws, nuts, etc.) in this BOM to optimize manufacturability.

P/N	DESCRIPTION	QTY	REF
	UL CONFIGURATION		
7-51-1219	SHEET WELCOME-TO-ALESIS-FAMILY 5 x 8"	1	
	LITERATURE/PACKAGING		
4-71-0015	CABLE USB 2 METERS A/B	1	
7-22-0016	SOFTWARE CD UB0	1	
7-50-0200	STICKER BARCODE S/N UB0	1	
7-51-0173	REF MANUAL, UB0	1	
7-80-0391	BOX SHIPPING UB0	0.05	
7-80-0390	BOX GIFT UB0	1	
7-91-1002	GEL SILICA 5G PACKET	1	
7-94-xxxx	POLYBAG	1	
LABOR	LABOR	1	FINAL ASSY AND TESTING
	TOP LEVEL MECHANICALS		
TBD BY VENDOR	SCREWS, MISC	18	
9-01-0088	CHASSIS EXTRUDED ALUMINUM UB0	1	
9-11-0053	COVER REAR PANEL MOLDED PLASTIC UB0	1	
9-11-0054	COVER FRONT PANEL MOLDED PLASTIC UB0	1	
9-15-0405	LENS TINTED PLASTIC UB0	1	
9-15-0406	KNOB PLASTIC ELECTROPLATED UB0	5	
9-23-0018	FOOT RUBBER DOME CA	4	
	TOP LEVEL ELECTRICALS		
9-79-0350	**ASSY PCB MAIN UB0**	**1**	
9-79-0378	**ASSY PCB FRONT PANEL UB0**	**1**	
9-79-0350	***ASSY PCB MAIN UB0***		
0-15-0101	RES 100 OHM 1/10W 5% 0805	8	R1-2 R4 R24 R66 R93 R104 R115
0-15-0109	RES 1.0 OHM 1/10W 5% 0805	10	R12-15 R42-45 R97 R119
0-15-0152	RES 1.5K OHM 1/10W 5% 0805	1	R17
0-15-0153	RES 15K OHM 1/10W 5% 0805	8	R34-37 R51-52 R54-55
0-15-0221	RES 220 OHM 1/10W 5% 0805	2	R9 R101
0-15-0331	RES 330 OHM 1/10W 5% 0805	3	R11 R61 R71
0-15-0473	RES 47K OHM 1/10W 5% 0805	7	R38-39 R56-57 R98-100
0-15-0514	RES 510K OHM 1/10W 5% 0805	1	R47
0-15-0750	RES 75 OHM 1/10W 5% 0805	1	R16
0-16-1001	RES 1.00K OHM 1/10W 1% 0805	11	R3 R5-6 R18 R20-21 R23 R85-86
0-16-1002	RES 10.0K OHM 1/10W 1% 0805	11	R7 R25-26 R28-29 R41 R48 R65 R69
0-16-1003	RES 100K OHM 1/10W 1% 0805	16	R27 R32-33 R40 R49-50 R53 R68 R79
0-16-1182	RES 11.8K OHM 1/10W 1% 0805	2	R134-135
0-16-1211	RES 1.21K OHM 1/10W 1% 0805	8	R67 R76-77 R88-89 R91 R94-95
0-16-1302	RES 13.0K OHM 1/10W 1% 0805	2	R121-122
0-16-1829	RES 18.2 OHM 1/10W 1% 0805	2	R78 R90
0-16-2001	RES 2.00K OHM 1/10W 1% 0805	5	R10 R60 R64 R70 R74
0-16-2749	RES 27.4 OHM 1/10W 1% 0805	2	R19 R22

0-16-2941	RES 2.94K OHM 1/10W 1% 0805	2	R125-126	
0-16-3321	RES 3.32K OHM 1/10W 1% 0805	9	R30-31 R84 R108 R113 R117 R120	
0-16-3402	RES 34.0K OHM 1/10W 1% 0805	2	R124 R127	
0-16-3831	RES 3.83K OHM 1/10W 1% 0805	2	R133 R136	
0-16-3921	RES 3.92K OHM 1/10W 1% 0805	5	R46 R62-63 R72-73	
0-16-5361	RES 5.36K OHM 1/10W 1% 0805	2	R129-130	
0-16-6811	RES 6.81K OHM 1/10W 1% 0805	2	R114 R118	
0-16-7501	RES 7.50K OHM 1/10W 1% 0805	8	R81-83 R87 R105-107 R111	
0-17-0101	RES CHIP ARRAY 4 X 100 OHM 1/16W 5% ISOLATED C-C=0.8mm	4	R8 R58-59 R103	
1-07-0224	CAP 2200uF ELEC 20% 6.3V 5x10.2x20mm	2	C66 C81	
1-08-0222	CAP 22uF ELEC 16V 20% 1.5x4x7mm	34	C5 C8-9 C14-15 C19 C23 C37 C39-40	
1-12-0472	CAP 47uF ELEC 20% 63V 2.5x6.3x11mm	5	C25-26 C30-31 C35	
1-16-1103	CAP 100uF ELEC LOW-ESR 20% 35V 105øC 2.5x6x11mm	3	C17 C32-33	
1-55-0189	CAP 18pF NPO 0805	3	C104 C108-109	
1-55-0222	CAP 2200pF NPO 0805 50V	6	C111 C125-129	
1-55-0223	CAP 0.022uF X7R 0805 50V	1	C134	
1-55-0470	CAP 47pF NPO 0805 50V	4	C94-95 C118 C131	
1-55-0471	CAP 470pF 5% NPO 0805 50V	24	C87-92 C96-97 C99-102 C105-106	
1-56-0101	CAP 100pF NPO 0805 5% 50V	9	C93 C98 C107 C113 C116-117 C121	
1-56-0102	CAP 1000pF NPO 0805 5% 100V	5	C103 C110 C130 C135-136	
1-56-0104	CAP 0.1uF X7R 0805 10% 50V	40	C1-4 C6-7 C10-13 C16 C18 C20-22	
1-56-0150	CAP 15pF NPO 0805	4	C119-120 C132-133	
1-71-3102	CAP 10uF TANT-B 16V	2	C28-29	
2-50-4148	DIODE SIGNAL LS4148 MELF	11	D2-12	
2-51-0140	DIODE POWER SCHOTTKY MBRS140LT3 40V 1A	1	D1	
2-51-4401	TRANS NPN 2N4401 40V 1A SOT-23	2	Q3 Q5	
2-51-4403	TRANS PNP 2N4403 40V 800mA SOT-23	5	Q2 Q11-12 Q15-16	
2-54-0856	TRANS SMALL-SIGNAL PNP 65V 100mA BC856 SOT-23	4	Q6-9	
2-54-2114	TRANS SMALL-SIGNAL NPN 2SD2114K SOT-23	6	Q1 Q4 Q10 Q13-14 Q17	
2-54-6306	TRANS SMALL-SIGNAL DUAL P-CHAN EN-MOSFET FDC6306P ISOLATE	2	U6-7	
2-61-2985	IC REG VOLTAGE LP2985IM5-4.0 LDO 4V 150mA SOT23-5	1	U8	
2-61-3578	IC REG VOLTAGE IC REG VOLTAGE LM3578A ADJ 100KHz PWM SWITC	1	U10	
2-61-7223	REG VOLTAGE NJU7223DL1-33 3.3V TO-252	2	U1 U3	
2-62-0157	IC 74AHC157 QUAD 2-TO-1 LINE DEMUX SOP-16	1	U14	
2-65-0017	IC 74LVC1G17 SINGLE GATE SCHMITT-TRIG BUF	1	U5	
2-69-2464	IC EEPROM SERIAL 64K-BIT 24C64 SOIC-8	1	U12	
2-70-1020	IC MPU TAS1020B USB TQFP-48	1	U11	
2-71-3079	IC MC33079 QUAD-OP-AMP SOP-14	3	U13 U16 U18	
2-74-0181	IC OPTO-ISOLATOR TLP181 TRANS-OUT SMD	1	U2	
2-75-4265	IC CODEC CS4265 24-BIT STEREO LOW-POWER QFN-32	1	U4	
2-75-4344	IC CONVERTER D/A CS4344 24-BIT 192KHZ (I2S) TSSOP-10	1	U17	
2-84-8416	IC RECEIVER DIG AUDIO 192kHz CS8416 TSSOP-28	1	U15	
2-85-0403	IC VOLTAGE INVERTER CHARGE PUMP UNREG TPS60403 SOT23-5	1	U9	
4-00-0002	JACK DIN 5-PIN MIDI PCB MOUNT 180° W/SHIELD	2	J6-7	
4-01-0008	JACK RCA DUAL FEMALE PANEL-MNT/HOR-MNT	1	J2	
4-02-0010	JACK 1/4 4-PIN FEM PCB MNT 90-DEG	2	J4-5	
4-02-0011	JACK 1/4 STEREO 5-PIN FEM PCB-MNT VERT W/ BUSHING	4	J9-10 J12-13	
4-05-0025	JACK XLR 3-PIN FEM PCB-MNT VERT	2	J8 J11	
4-08-0402	CON USB 4-PIN FEMALE PC-MNT HORIZONTAL	1	J1	
4-14-1200	HEADER DIL 12-PIN 2mm MALE 90° SHRD	3	J14-16	
7-01-0048	CRYSTAL 6MHz PARALLEL 16pF HC-49US	1	X1	
7-20-0070	INDUCTOR FERRITE BEAD 120 OHMS @ 100MHZ 0805	2	L2-3	
7-20-0073	INDUCTOR POWER 330uH 0.61A 5x10.5x10.5mm	1	L1	
7-40-8865	TRANSFORMER 1-10 mHz PULSE 1:1	1	T1	
9-40-0350-B	PCB, MAIN UB0 REV B	1		
LABOR	LABOR	345		
9-79-0378	***ASSY PCB FRONT PANEL UB0***			
0-09-0046	POT 10KA DUAL VERT 15mm D-SHAFT	2	P3 P5	
0-09-0047	POT 10KB DUAL VERT 15mm D-SHAFT	1	P4	

0-09-0052	POT 5KC SINGLE VERT 15mm D-SHAFT	2	P1-2	
0-15-0100	RES 10 OHM 1/10W 5% 0805	2	R3 R5	
0-16-1001	RES 1.00K OHM 1/10W 1% 0805	2	R7-8	
0-16-1002	RES 10.0K OHM 1/10W 1% 0805	11	R2 R6 R17 R22-25 R27 R30 R34-35	
0-16-1003	RES 100K OHM 1/10W 1% 0805	8	R18-21 R28-29 R32-33	
0-16-1401	RES 1.40K OHM 1/10W 1% 0805	1	R10	
0-16-2941	RES 2.94K OHM 1/10W 1% 0805	1	R11	
0-16-3321	RES 3.32K OHM 1/10W 1% 0805	3	R1 R4 R12	
0-16-4752	RES 47.5K OHM 1/10W 1% 0805	1	R13	
0-16-4991	RES 4.99K OHM 1/10W 1% 0805	2	R26 R31	
0-16-5621	RES 5.62K OHM 1/10 1% 0805	1	R9	
0-17-0102	RES CHIP ARRAY 4 X 1K OHM 1/16W 5% ISOLATED c-c=0.8mm SMD	3	R14-16	
1-08-0222	CAP 22uF ELEC 16V 20% 1.5x4x7mm	14	C1 C3 C6-7 C12-16 C19-20 C22-24	
1-55-0471	CAP 470pF 5% NPO 0805 50V	2	C8-9	
1-56-0101	CAP 100pF NPO 0805 5% 50V	2	C2 C5	
1-56-0104	CAP 0.1uF X7R 0805 10% 50V	4	C4 C10-11 C18	
1-56-0150	CAP 15pF NPO 0805	2	C17 C21	
2-50-4148	DIODE SIGNAL LS4148 MELF	3	D7 D10-11	
2-71-3079	IC MC33079 QUAD-OP-AMP SOP-14	1	U4	
2-71-7082	IC NJU7082BM DUAL POWER OP-AMP LOW VOLTAGE SOP-8 0.2	1	U1	
2-72-0339	IC LM339 ANALOG COMP SOP-14	2	U2-3	
3-02-0057	LED GREEN 1.1mm X 3.4mm RECT	7	D5-6 D8-9 D12 D14-15	
3-02-0058	LED YELLOW 1.1mm X 3.4mm RECT	2	D3-4	
3-02-0059	LED RED 1.1mm X 3.4mm RECT	3	D1-2 D13	
4-02-0011	JACK 1/4 STEREO 5-PIN FEM PCB-MNT VERT W/ BUSHING	1	J2	
4-15-0406	HEADER SIL 4-PIN 2mm MALE SHRD	1	J1	
6-01-0011	SWITCH SLIDE DPDT 2MM-PITCH	5	S1-5	
x-xx-xxxx	HEADER DIL 12-PIN 2mm STAKED	3	J4-6	
x-xx-xxxx	HEADER 4-PIN SIL 2mm STAKED	1	J3	
9-40-0378-A	PCB, FRONT PANEL UB0 REV A	1		
LABOR	LABOR	94		